



POWER FLOW

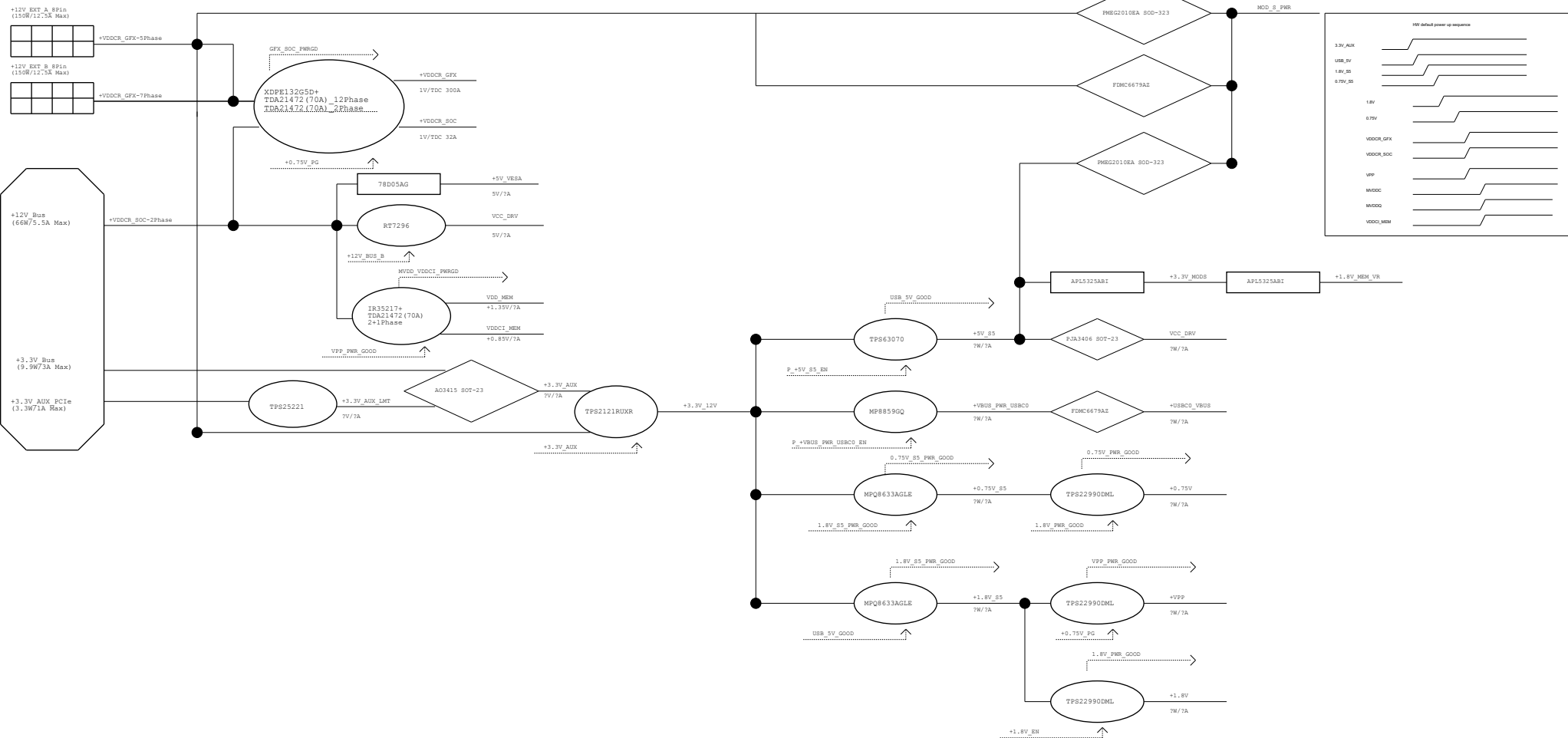
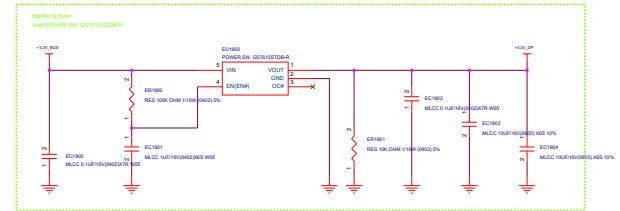
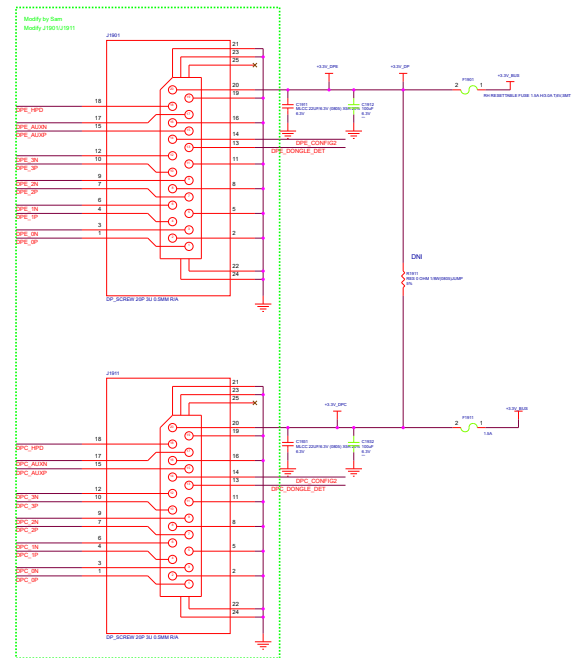
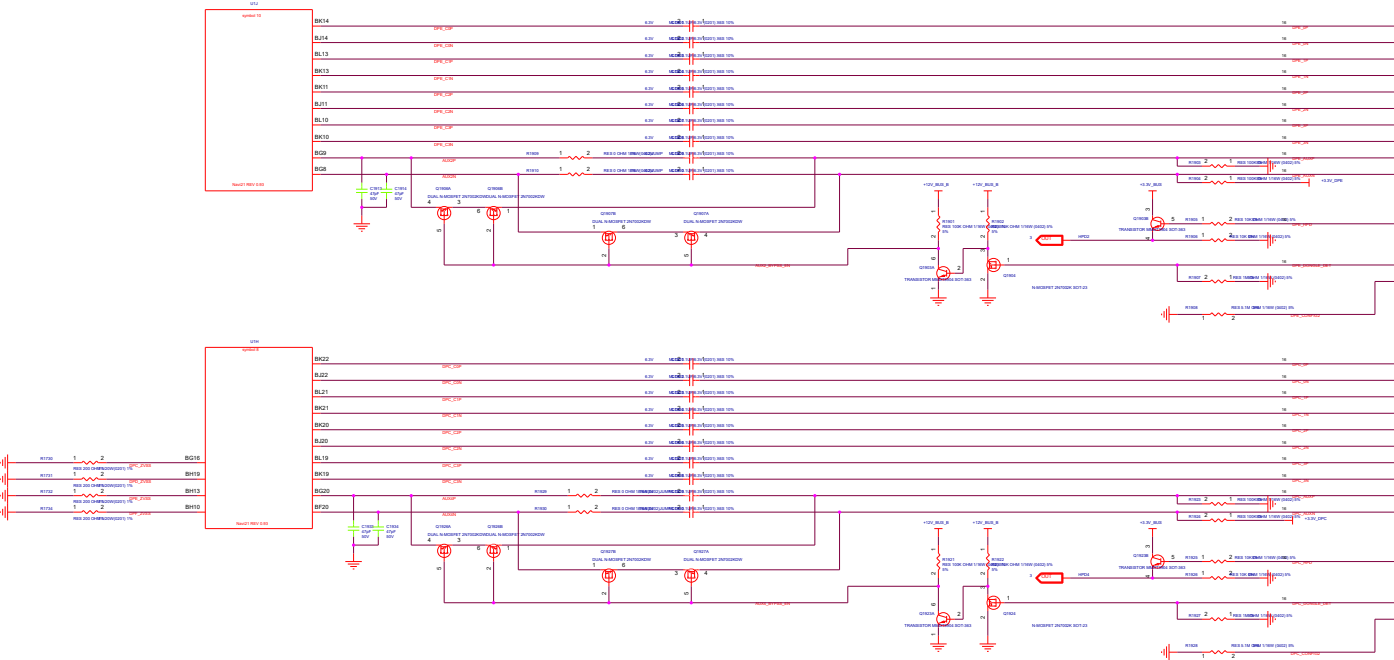
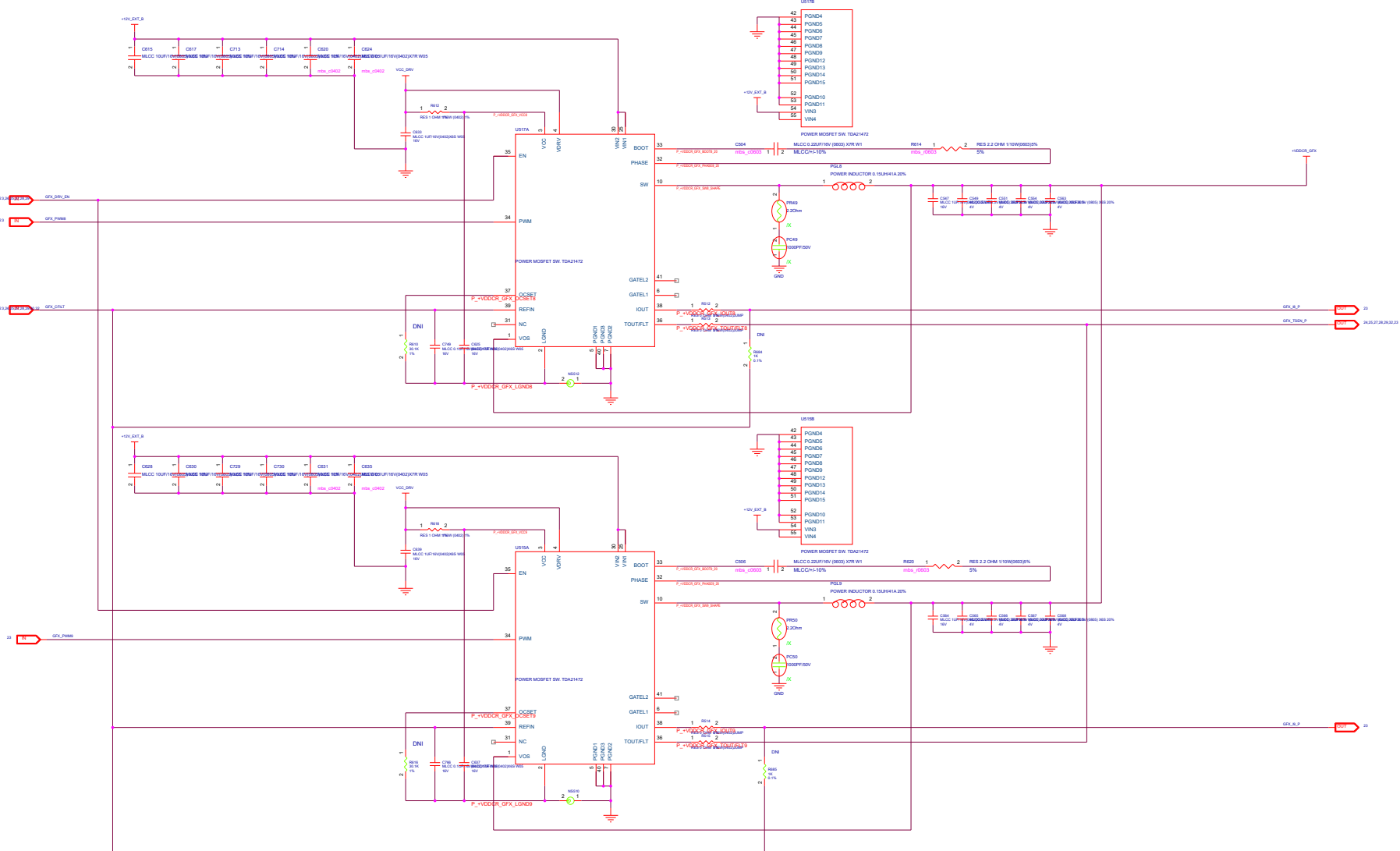


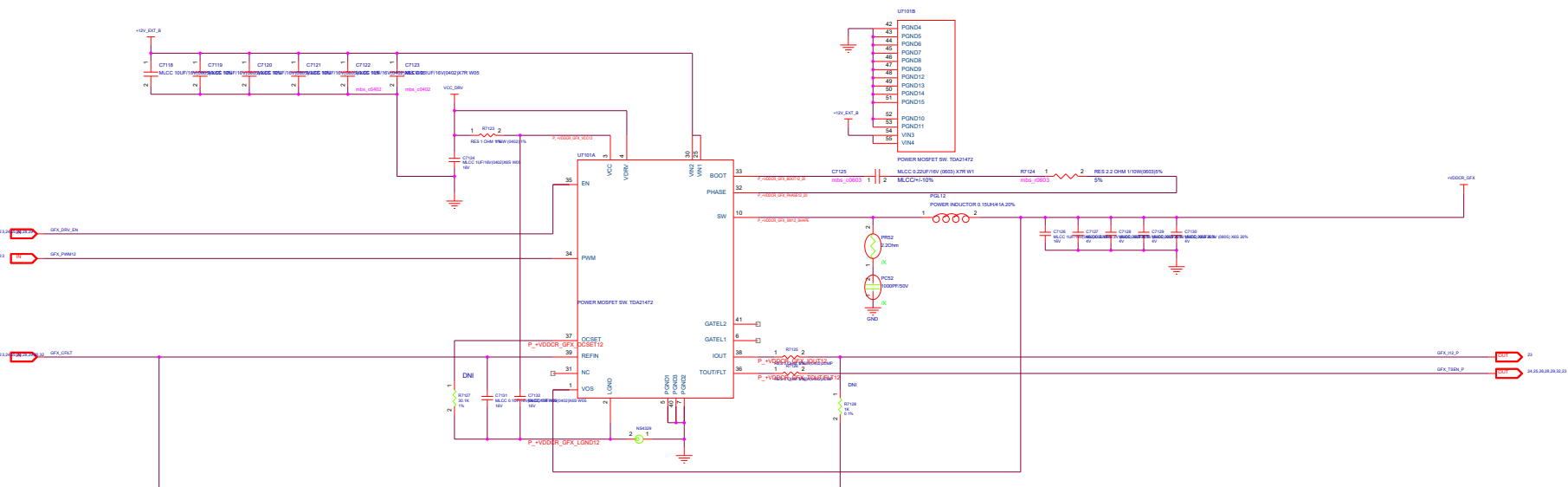
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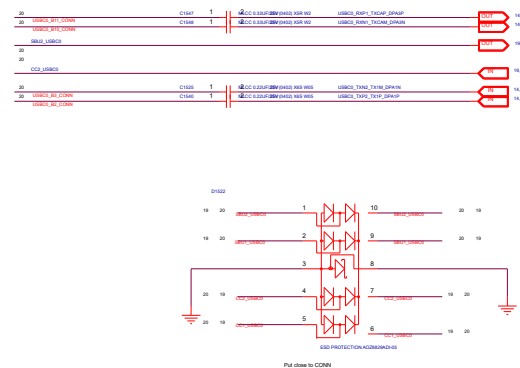
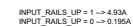
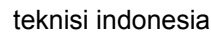
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1	TOC	26	GFX PHASES 8&9
2	NAVI 21 - PCIe Interface	27	GFX PHASES 11
3	NAVI 21 - GPIOs	28	GFX PHASES 5&7
4	NAVI 21 XTAL	29	GFX PHASES 3&10
5	XGMI	30	SOC PHASE 1&2
6	NAVI 21 MEM CH AB	31	VDD_MEM & VDDCI CONTROLLER
7	NAVI 21 MEM CH CD	32	VDD_MEM PHASES 1&2
8	NAVI 21 MEM CH EF	33	VDDCI_MEM PHASE 1
9	NAVI 21 MEM CH GH	34	NAVI 21 DECAPS
10	GDDR6 MEM CH CD	35	NAVI 21 POWER
11	GDDR6 MEM CH EF	36	NAVI 21 POWER and GND
12	GDDR6 MEM CH GH	37	POWER_MANAGEMENT
13	GDDR6 MEM CH AB	38	ClampWA
14	NAVI21 TMDPA - USB-C	39	SViZ & BxMACD
15	NAVI21 TMDPF - HDMI	40	THERMAL
16	NAVI21 TMOPC&E - DP	41	DPM_Status_LED & GDDR6_JTAG
17	NAVI21 TMDPA	42	PI Debug
18	NAVI21 USB	43	DEBUG
19	PD Controller	44	History
20	USB-C PORT 1		
21	USB_SV_1.8V_0.75V		
22	MODS CONTROL & POWER		
23	GFX & SOC CONTROLLER		
24	GFX PHASES 1&2		
25	GFX PHASES 4&6		

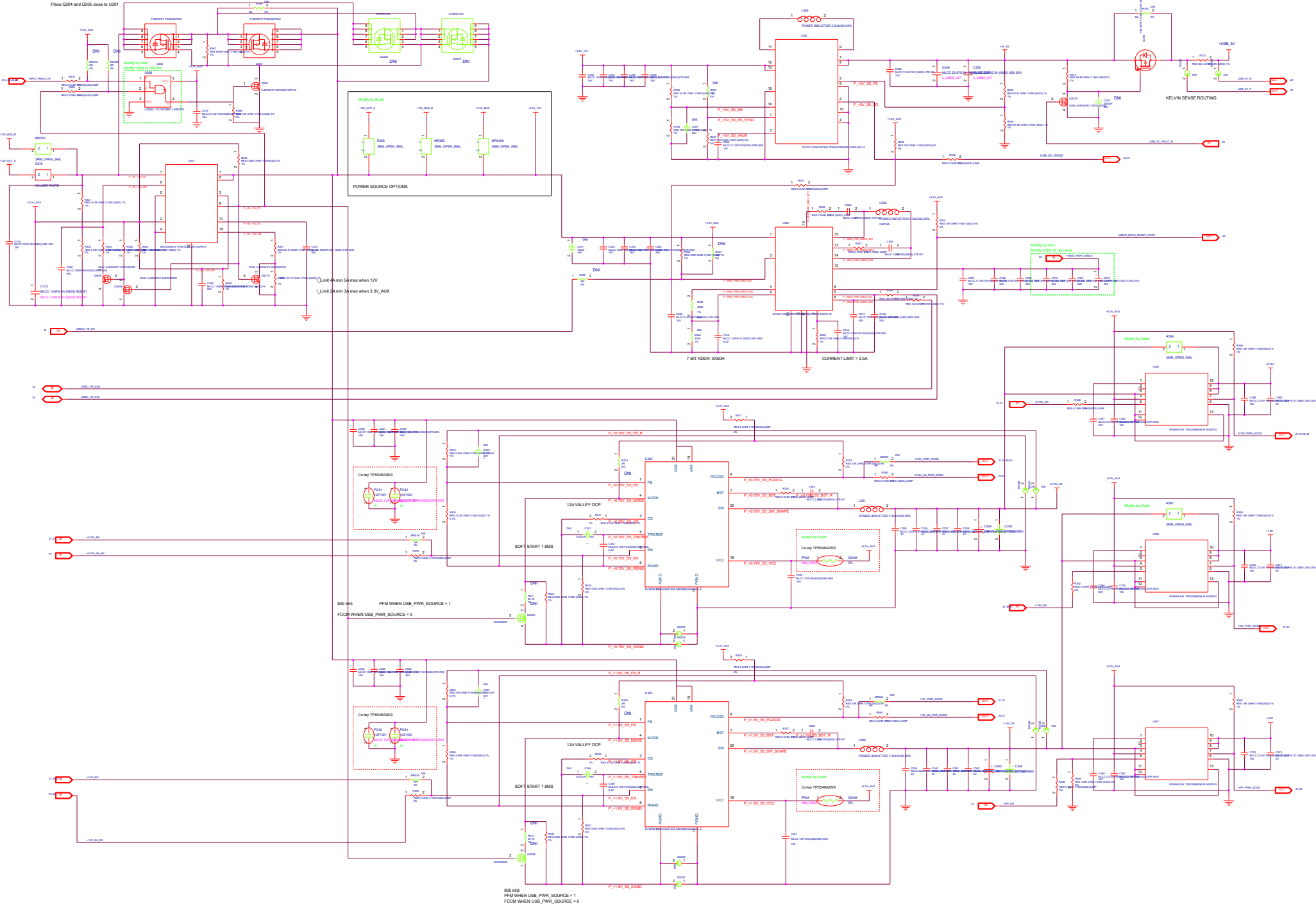


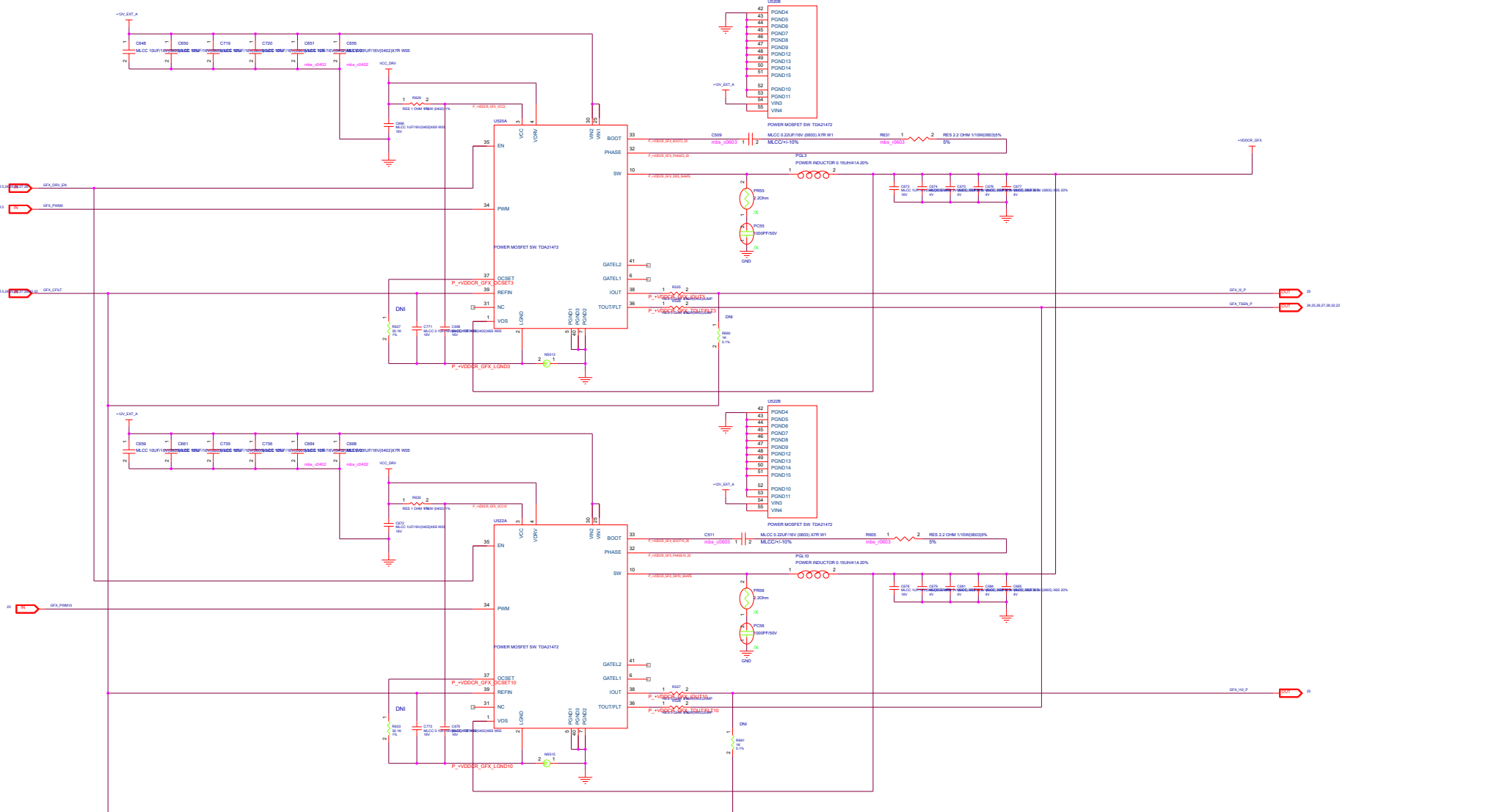




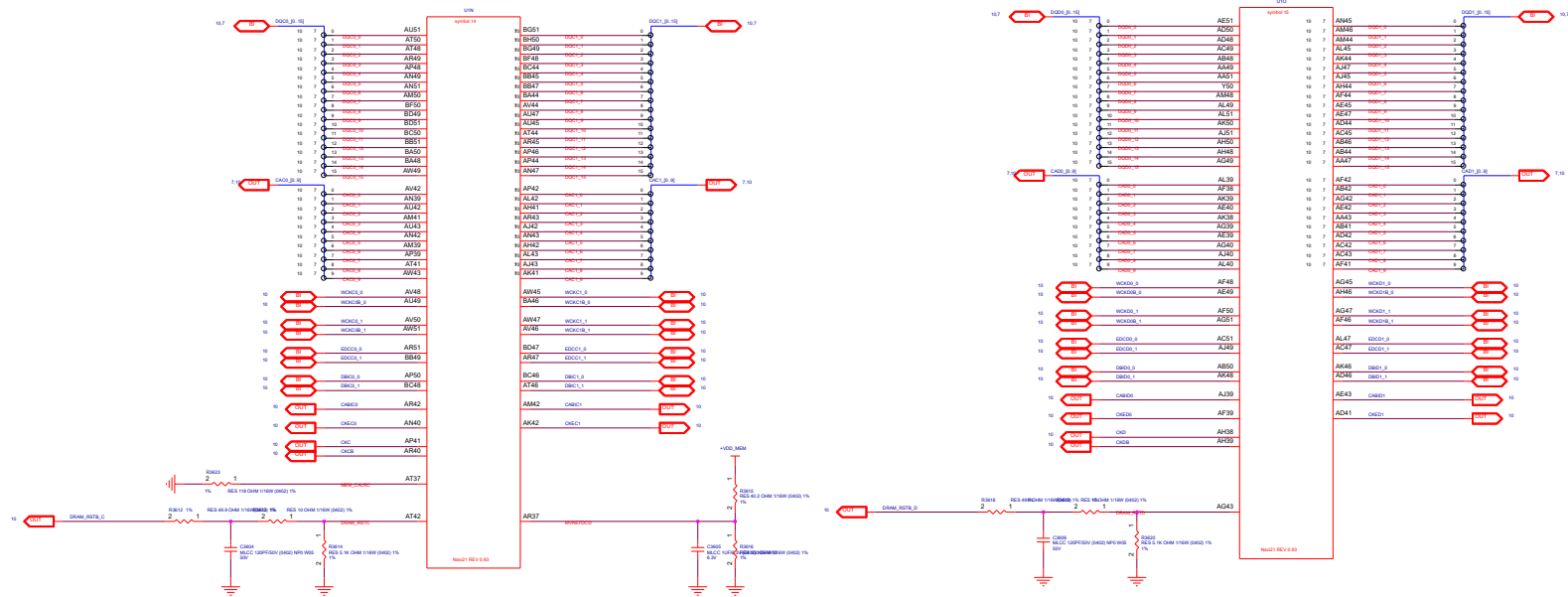


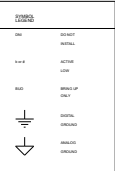


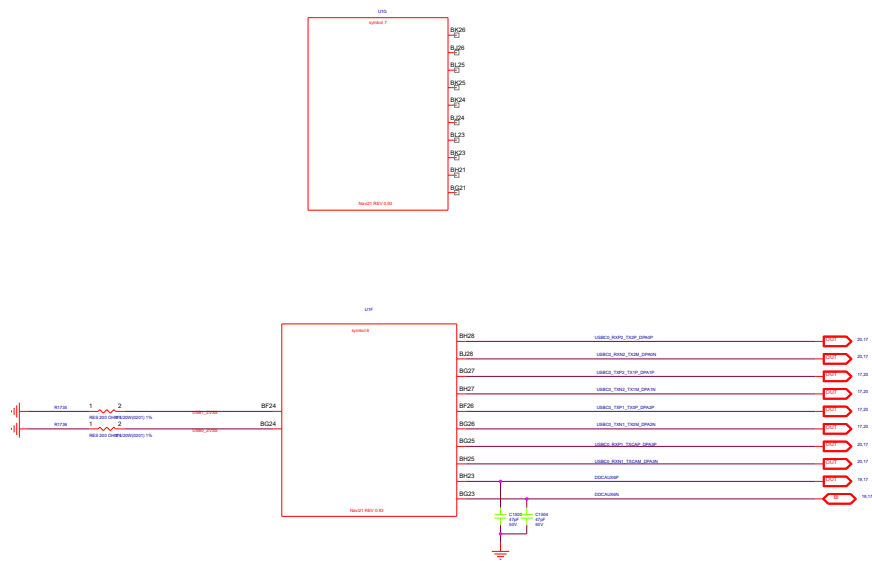


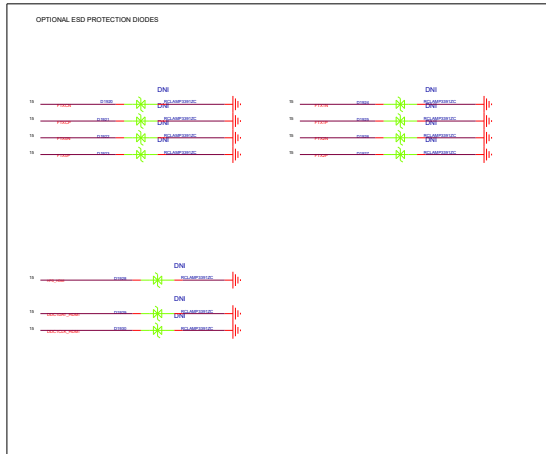
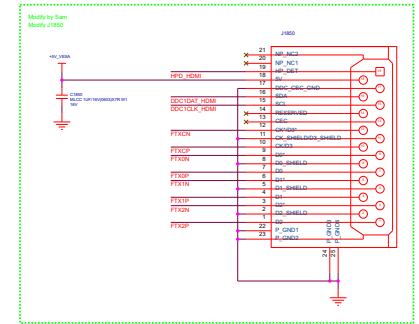
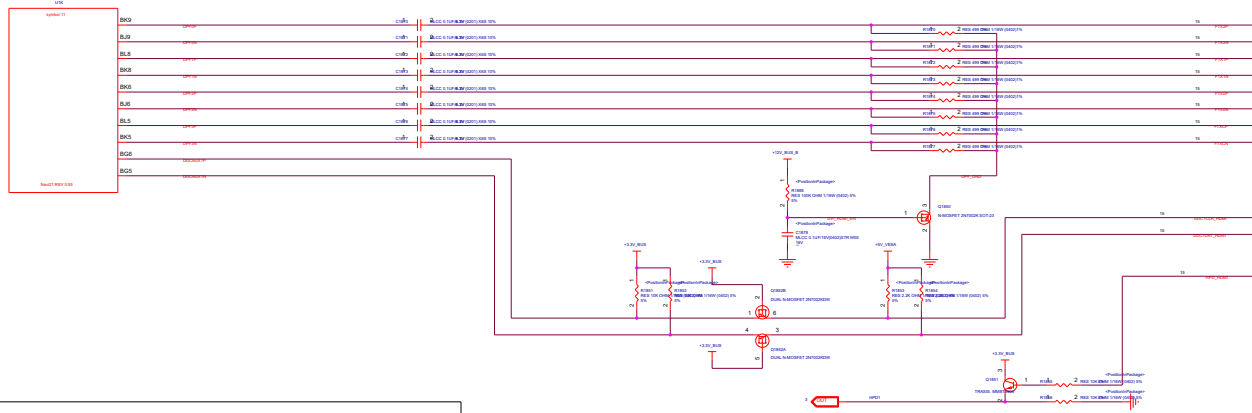
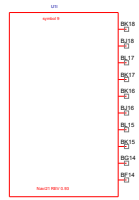


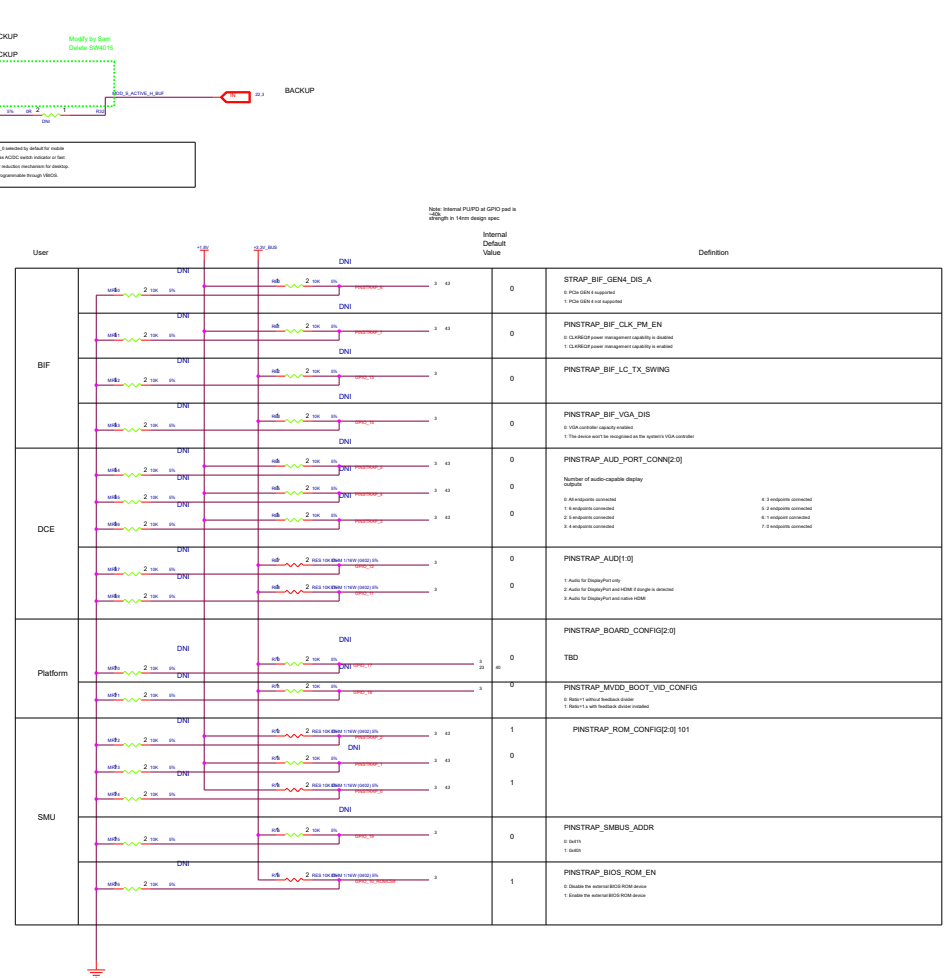


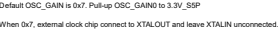


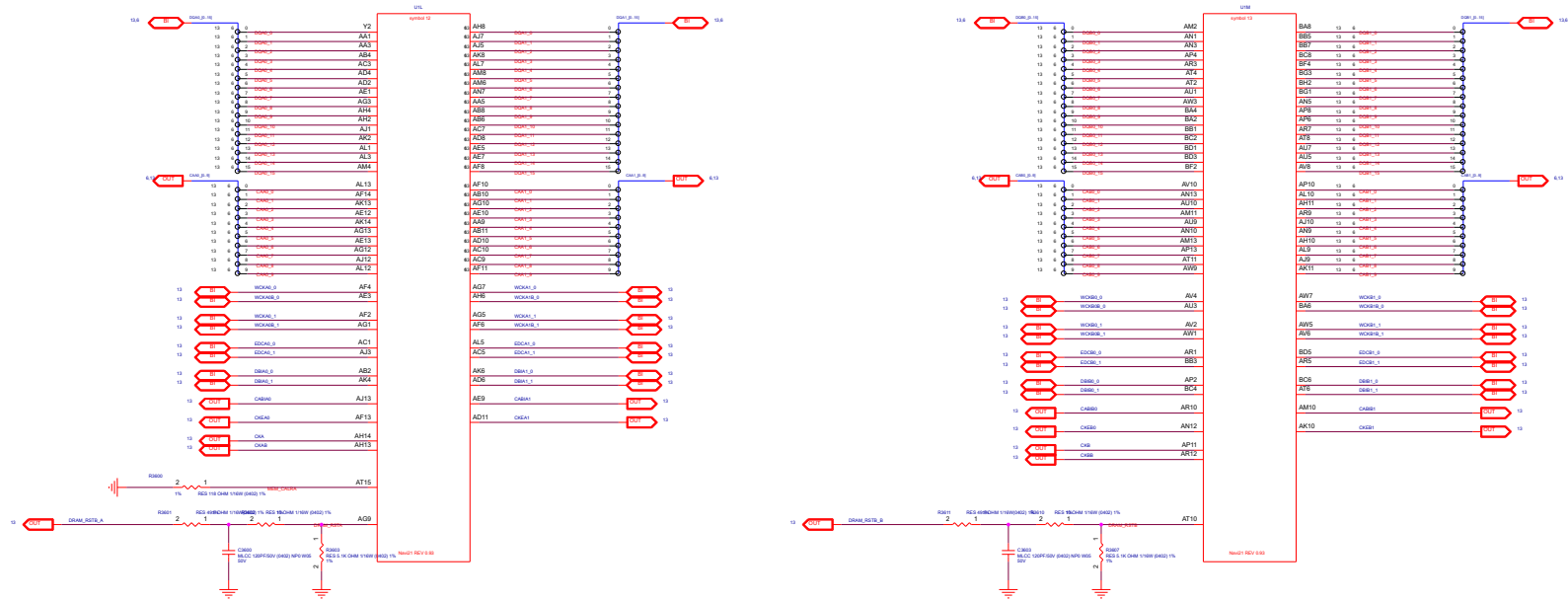


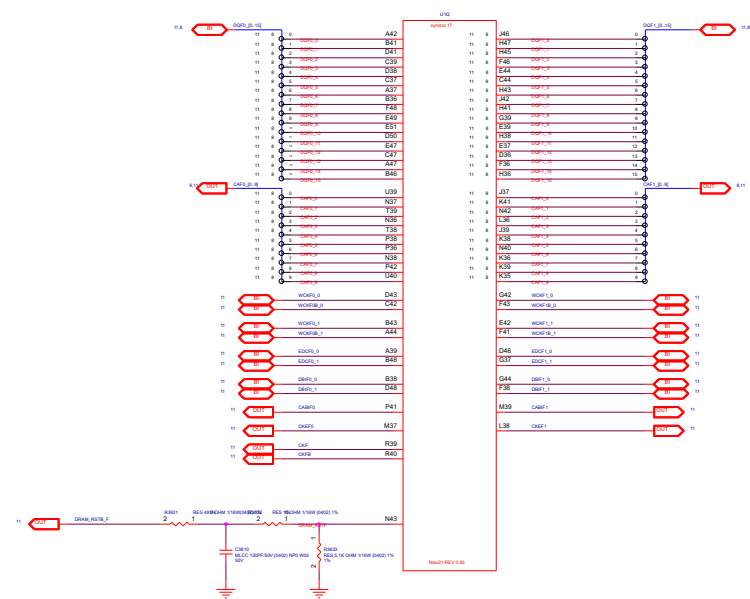


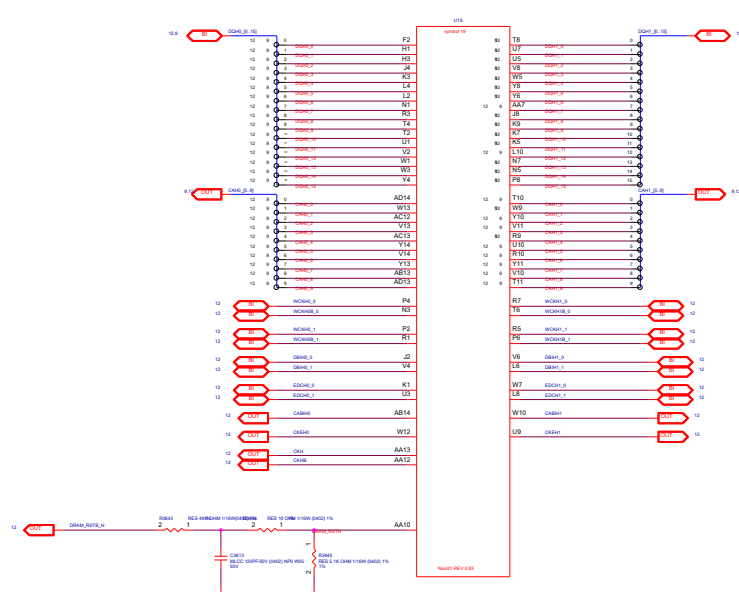






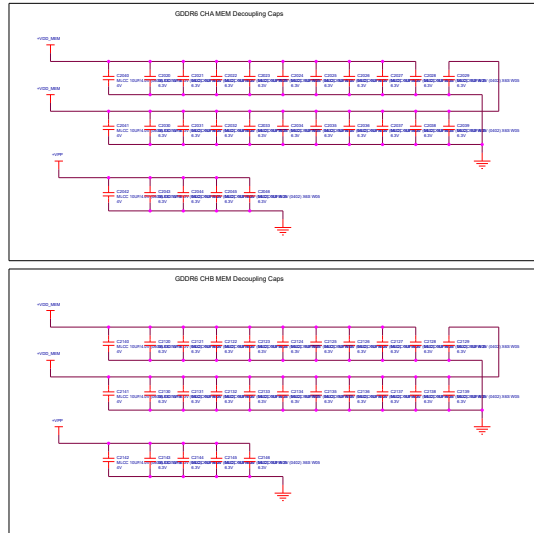
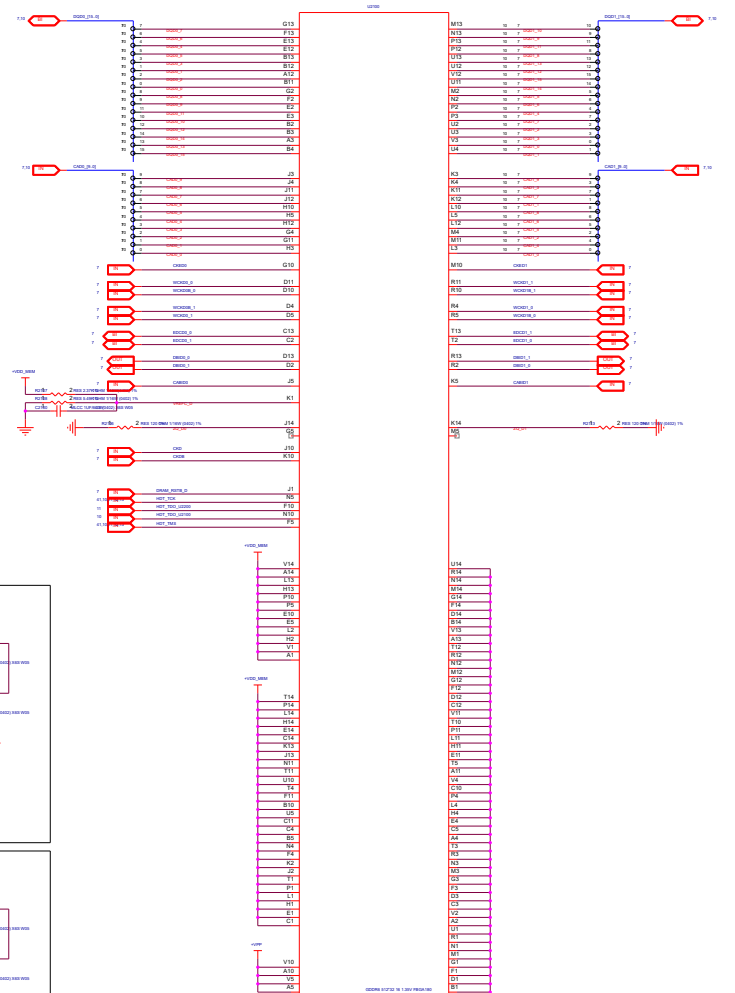
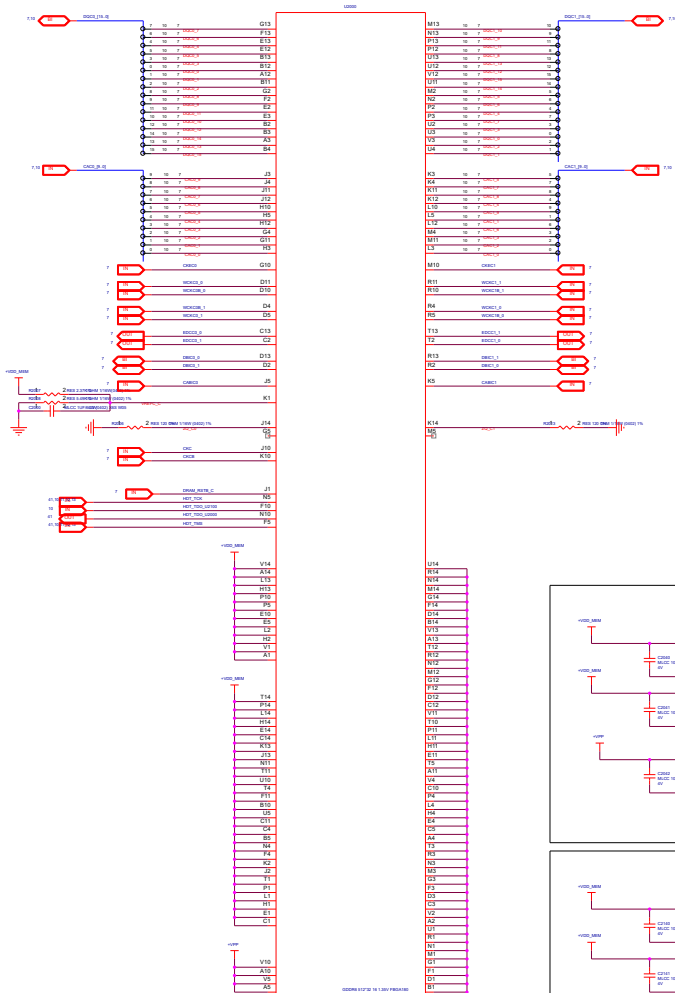




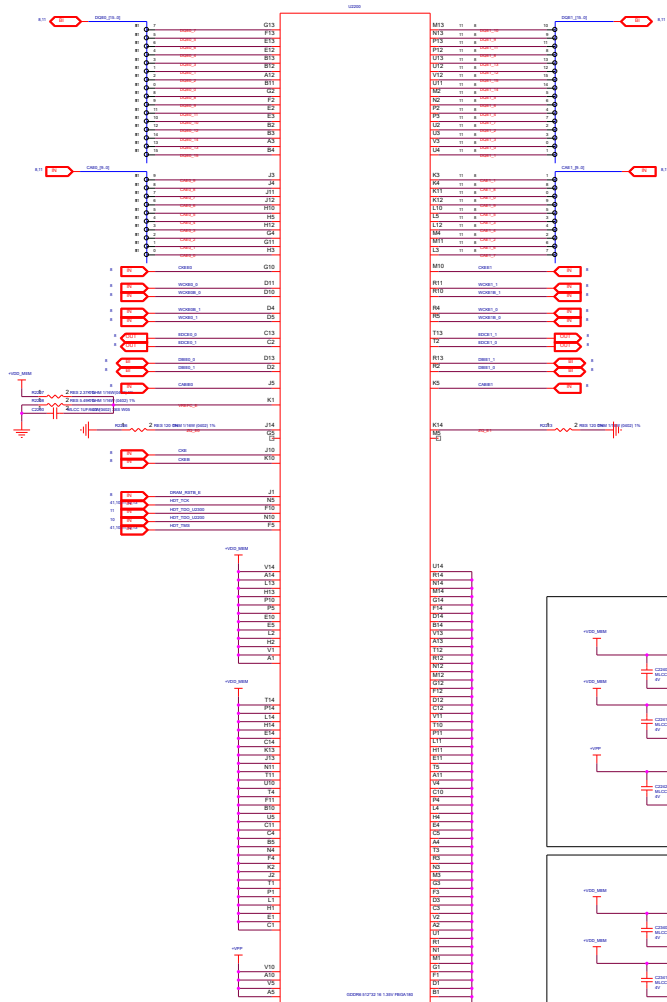


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ASIC CH1 -> MEM CHB

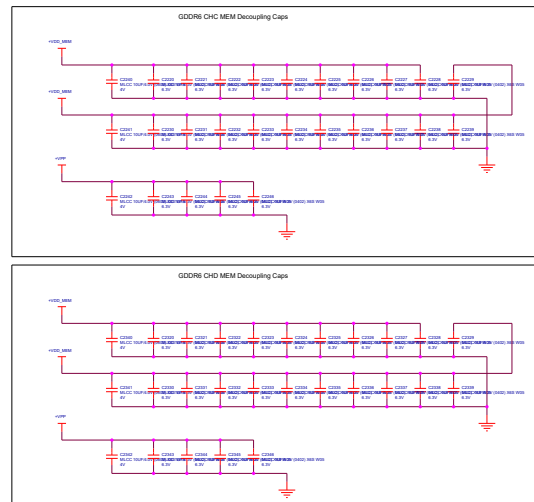
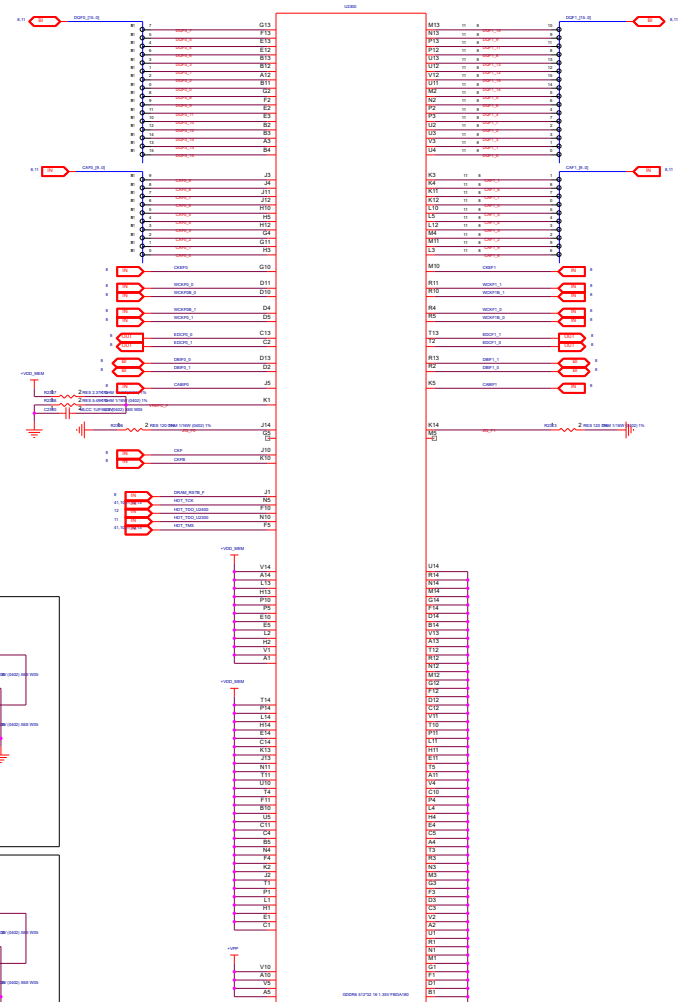
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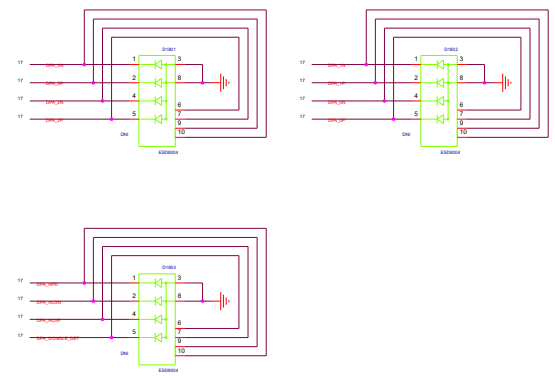
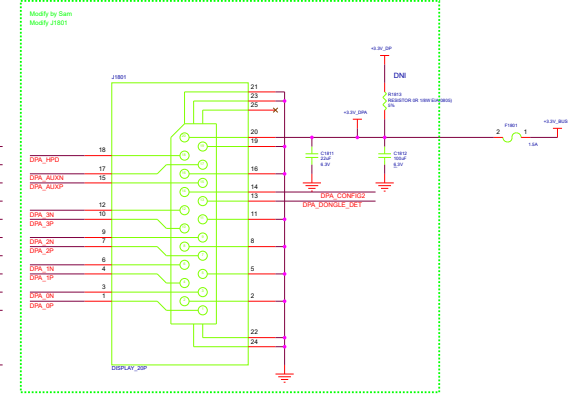
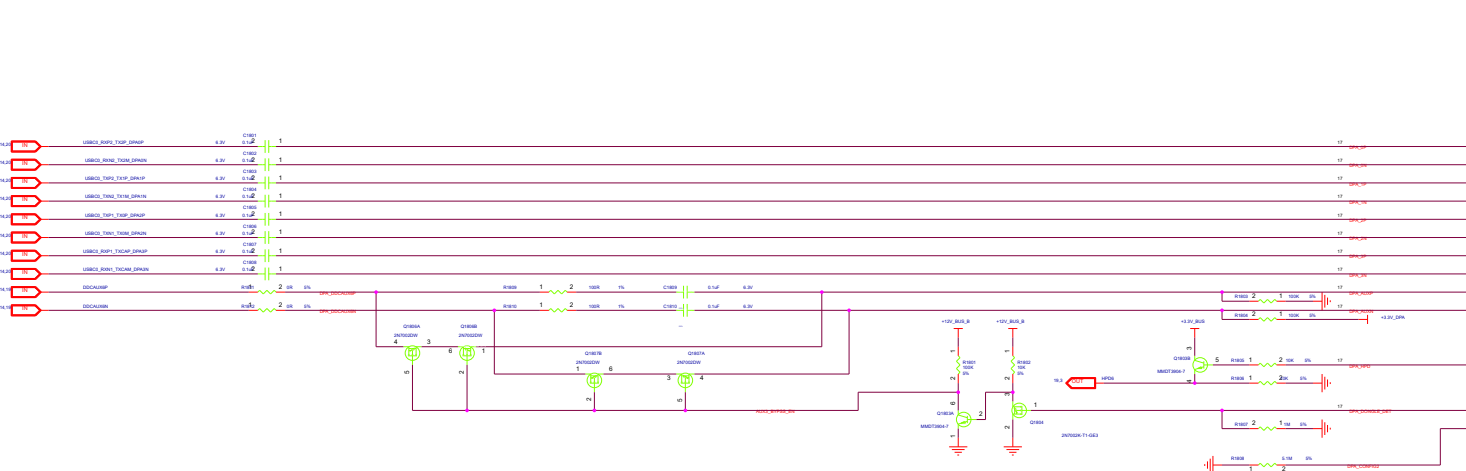


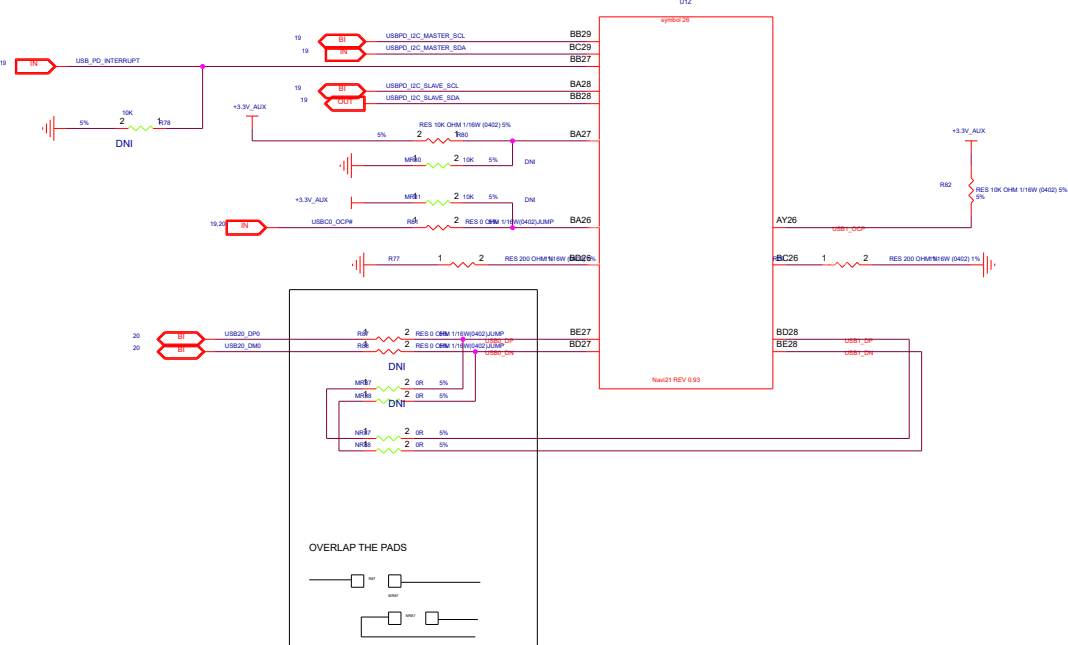
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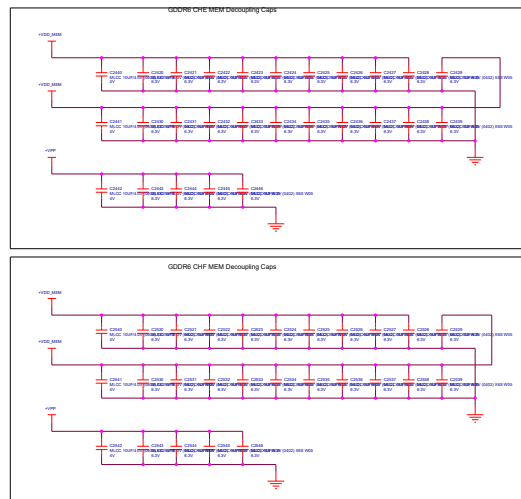
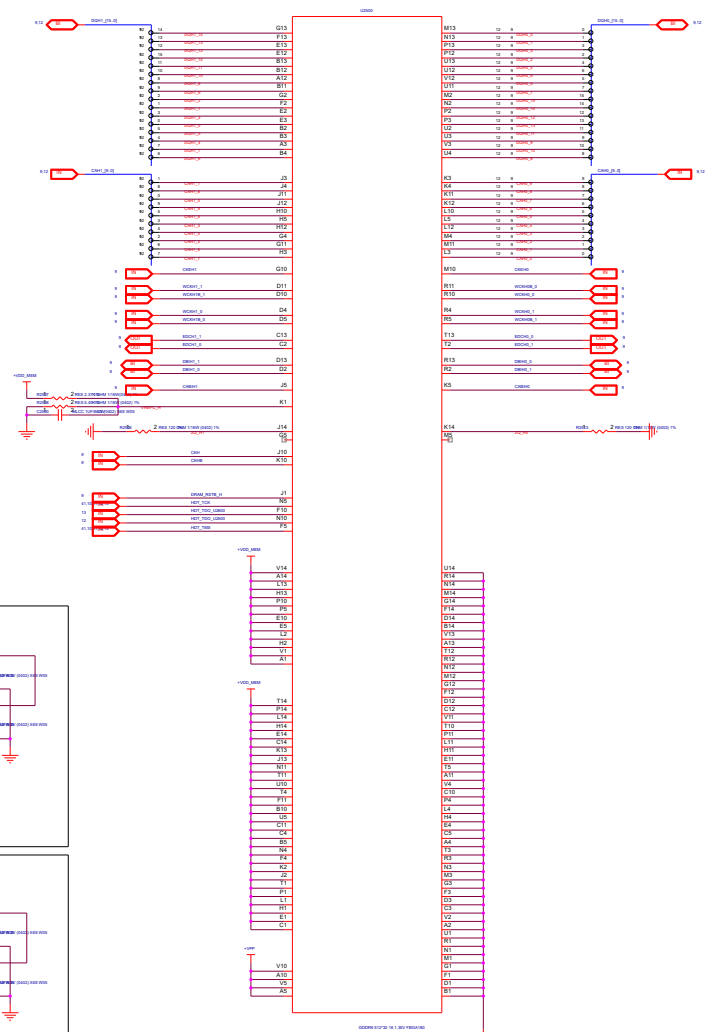


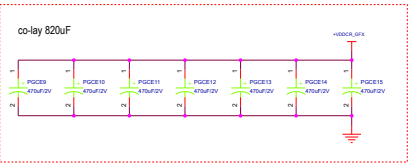
ASIC CH0 -> MEM CHA
ASIC CH1 -> MEM CHB



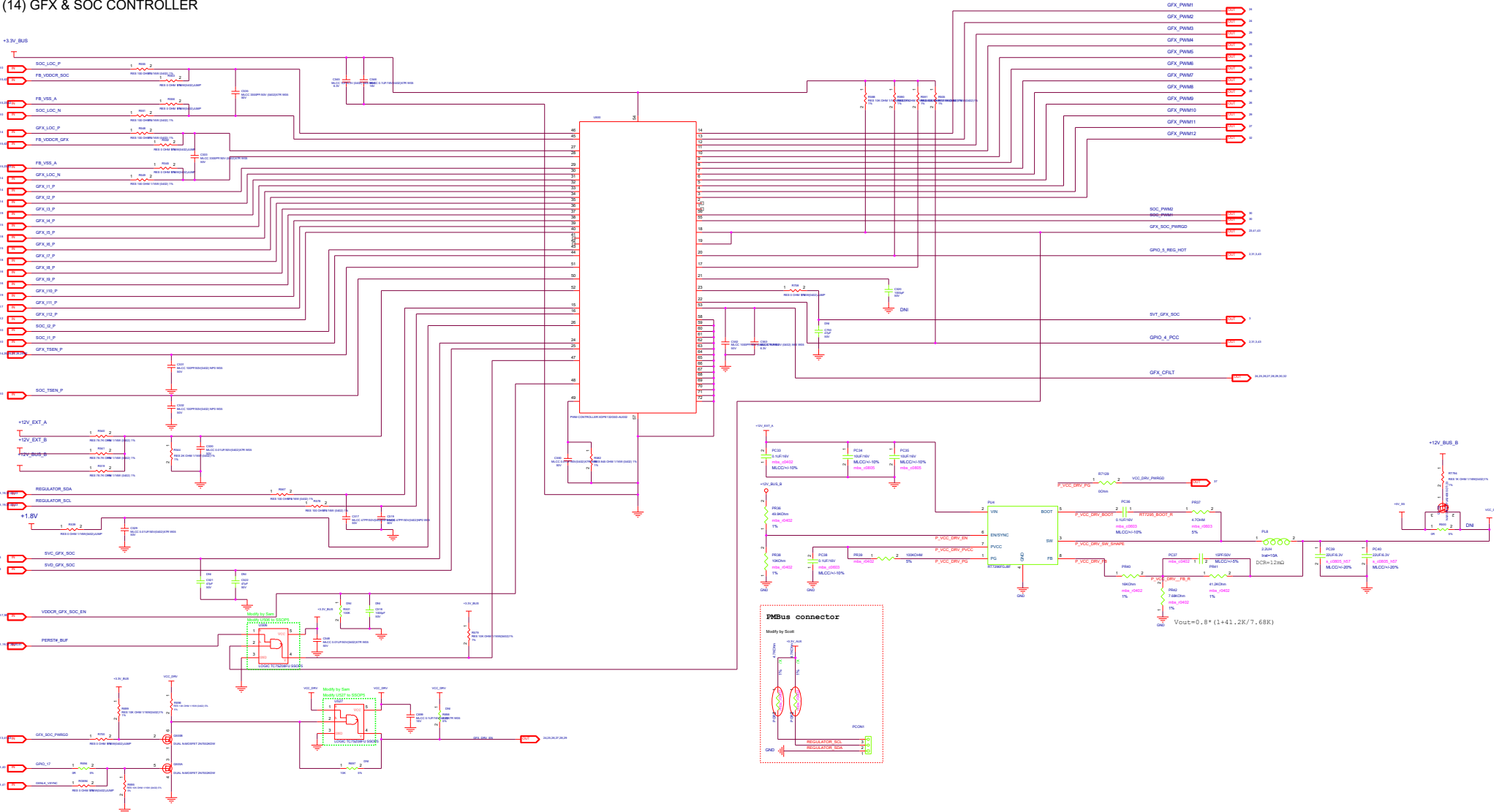


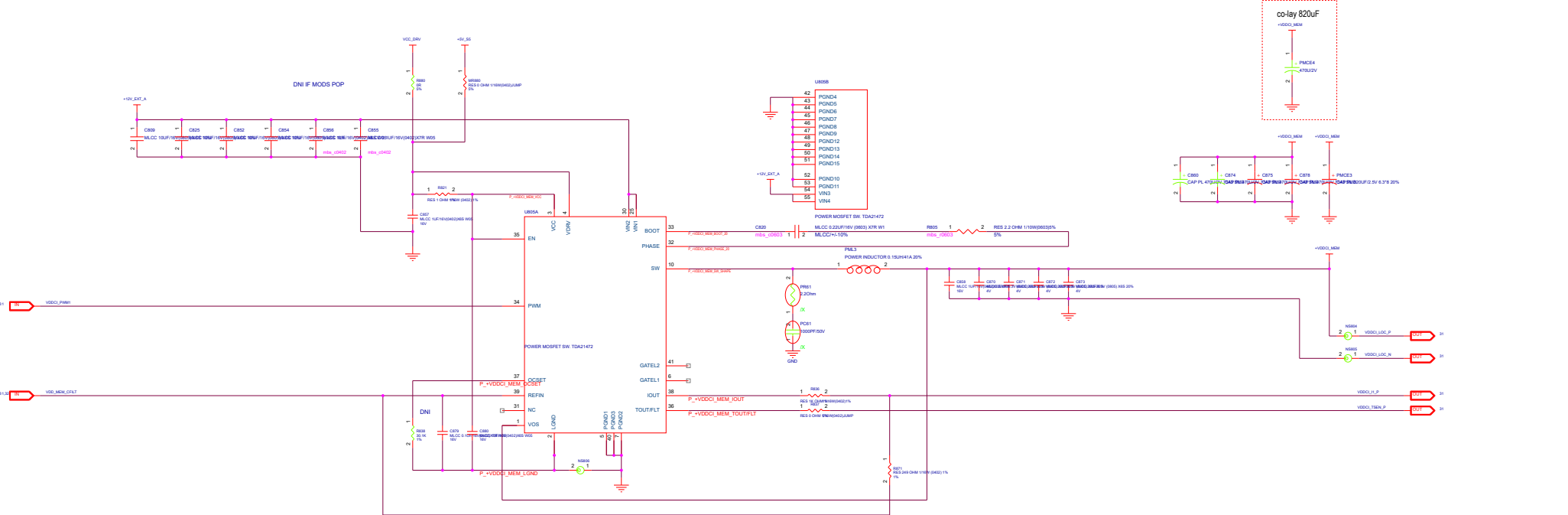


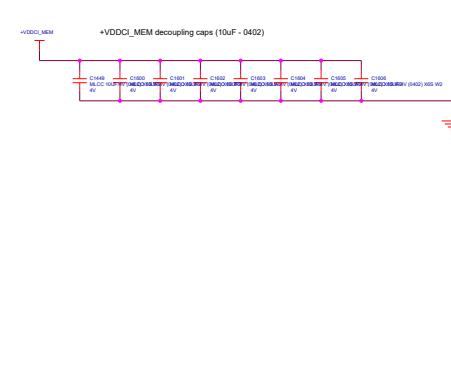
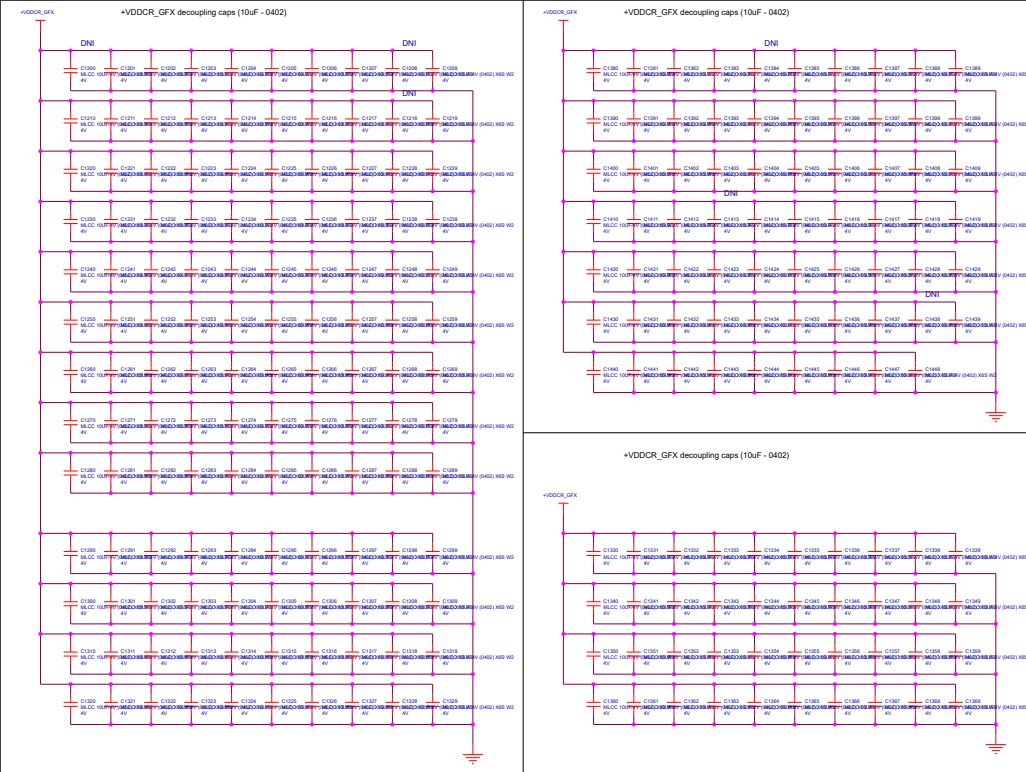




(14) GFX & SOC CONTROLLER

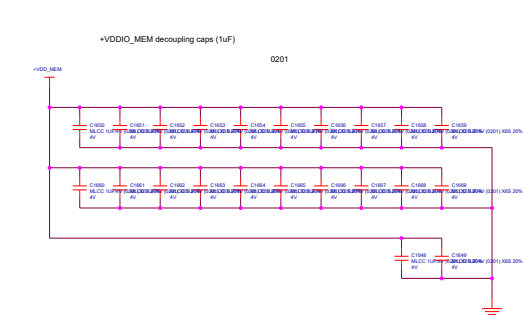
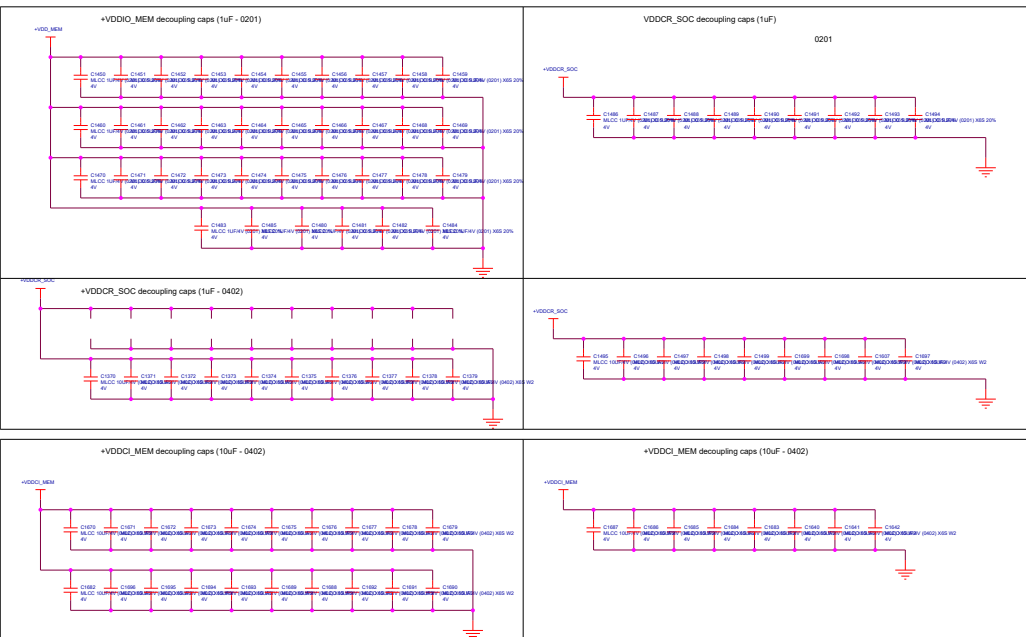


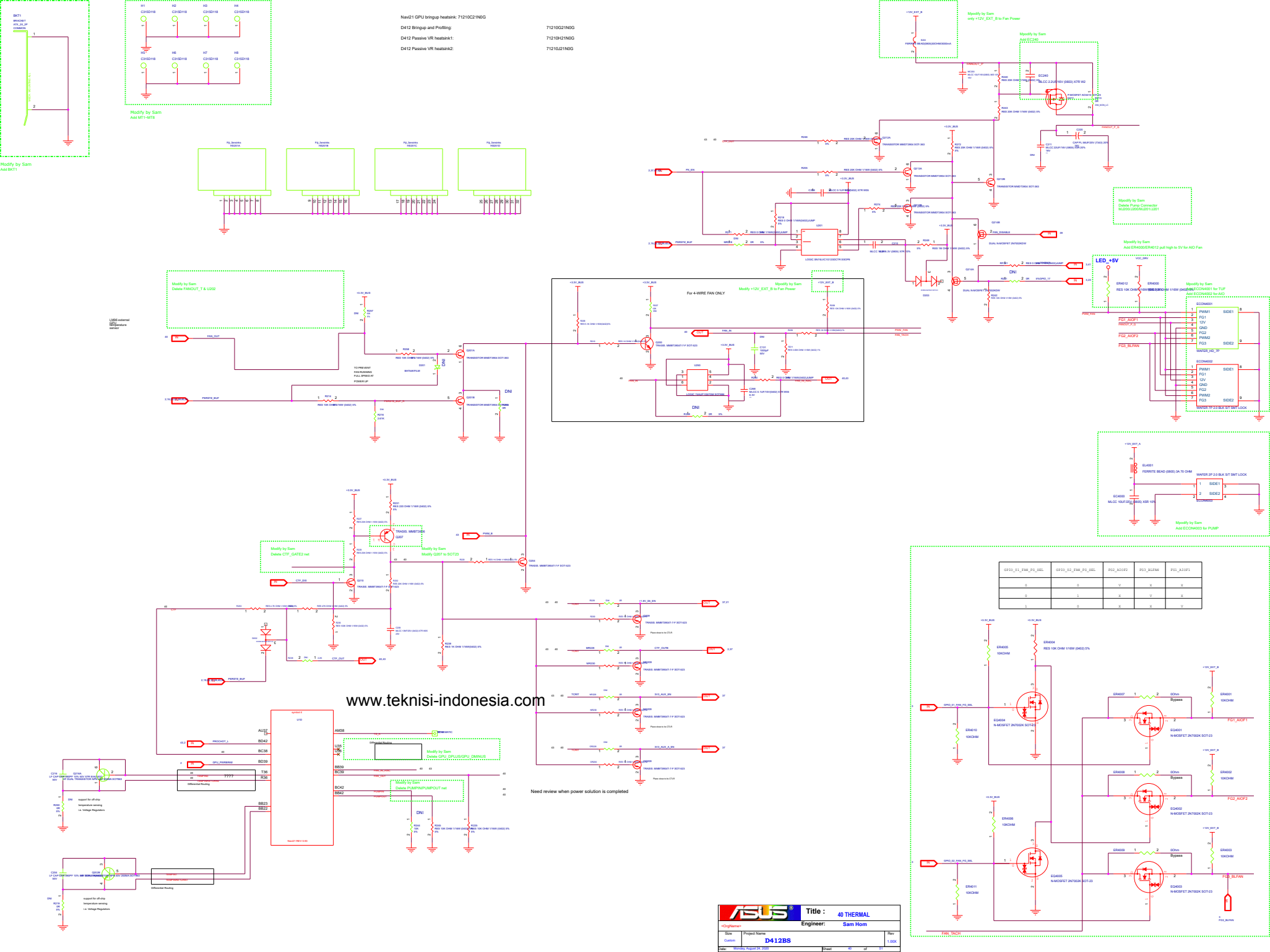


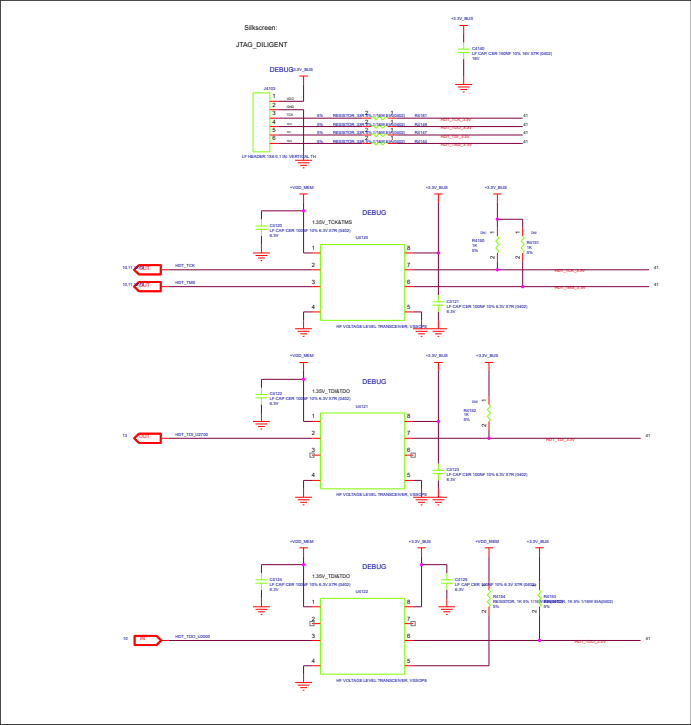


DNI these six caps to match SLT board and keep the design consistent across SKUs

- C1218
- C1208
- C1200
- C1438
- C1413
- C1384







Modify by Sam
Delete DPM LED

Modify by Sam
Delete FDS LED header
Delete RADEON Lightbar header

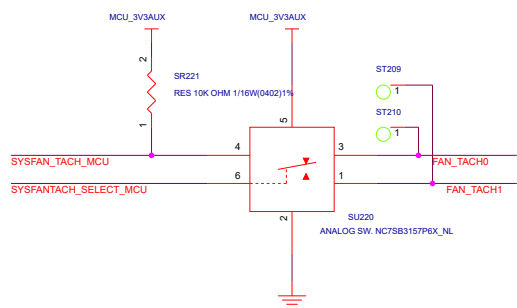
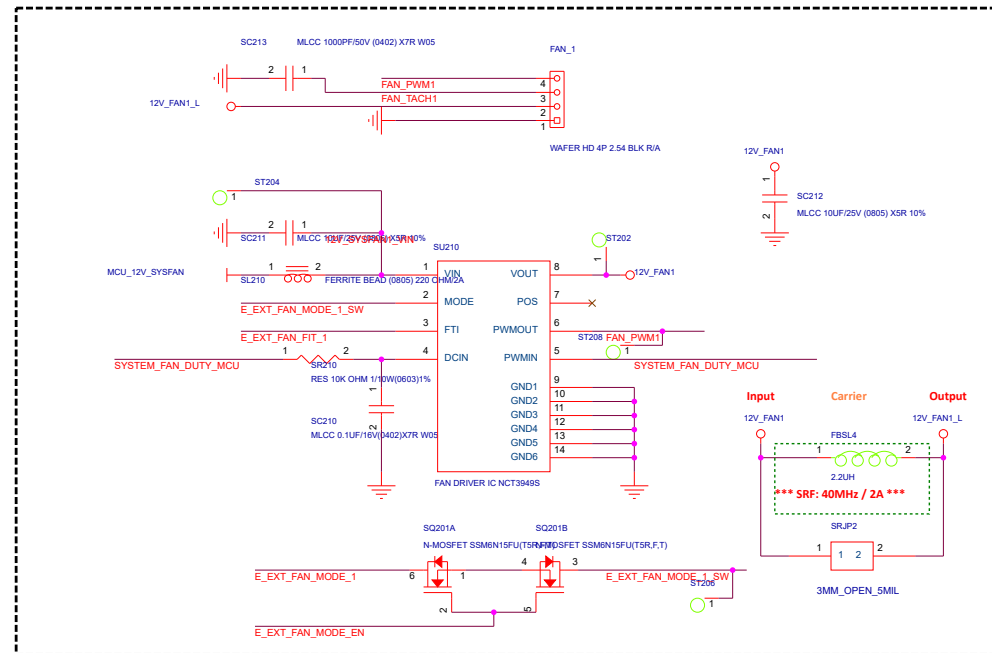
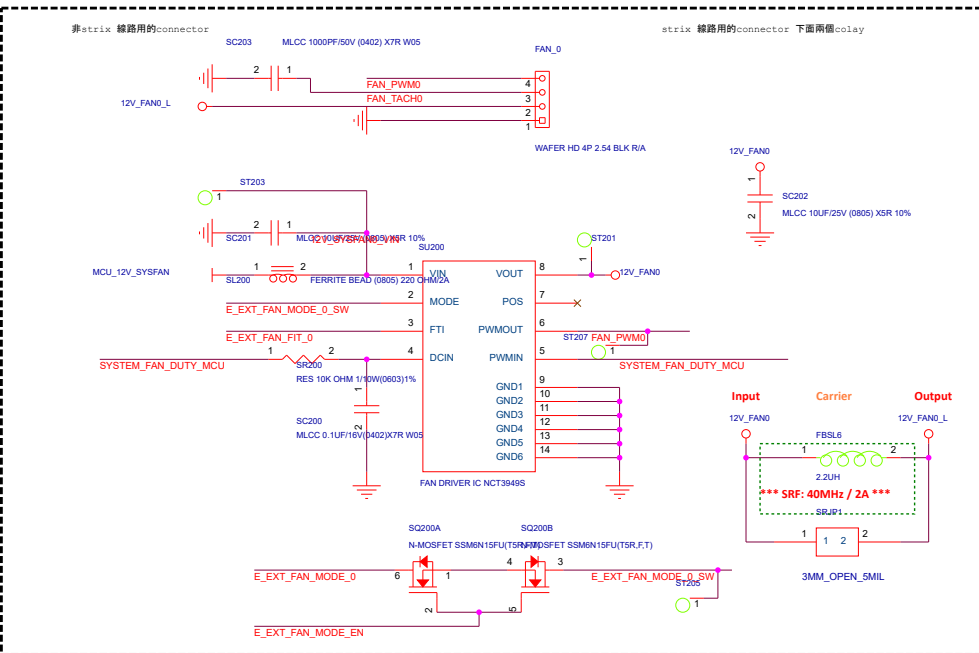
FOR PI DAUGHTER CARD

Modify by Sam

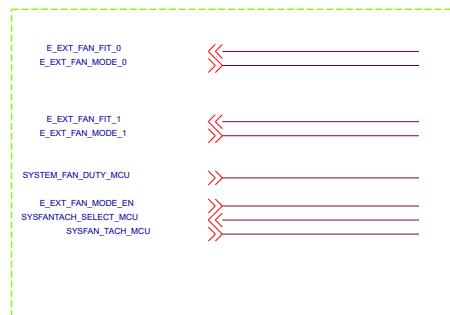
Delete PI DAUGHTER CARD

1	40B	Dec 11 2018	Added MOSFET circuit
1	40C	Jan 21 2019	Commented +1.8V_50 to OSC_VDD18 Added +0.8V_50 to OSC_VDD18 Added +0.8V_50 to OSC_VDD18 Added +0.8V_50 to OSC_VDD18

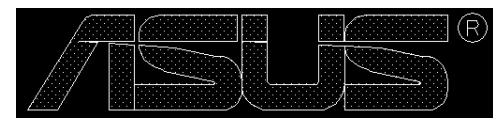
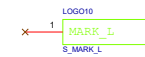
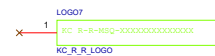
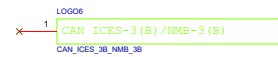
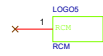
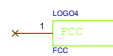
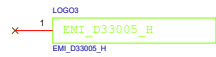
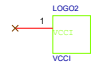
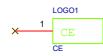
0002 SYSTEM FAN CONTROL



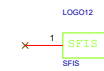
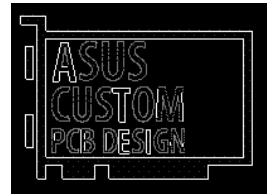
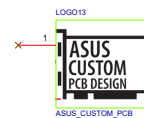
Fan Control II

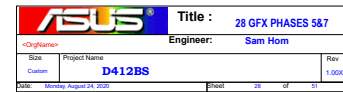


ASUS VGA PCB Logo

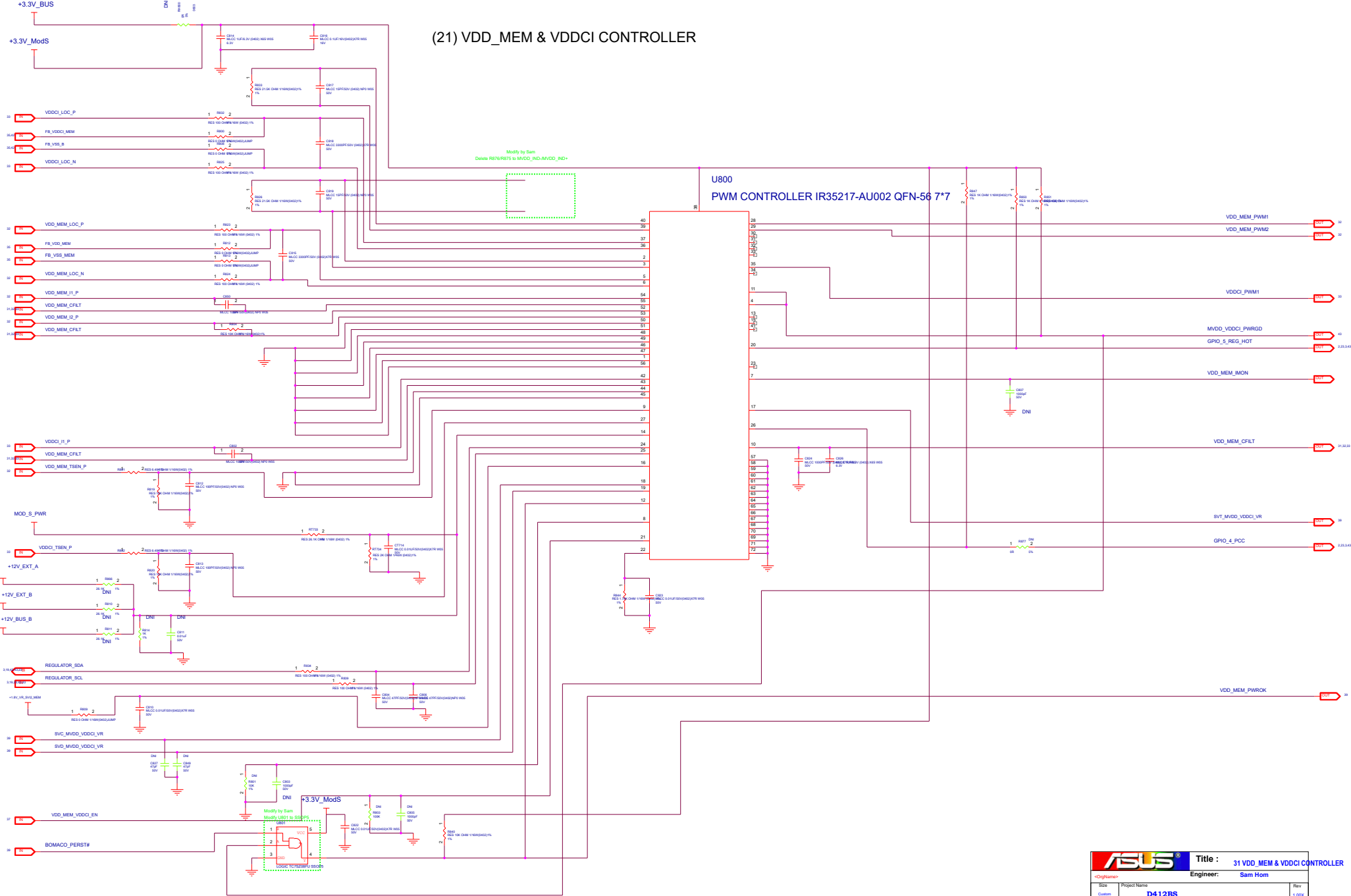


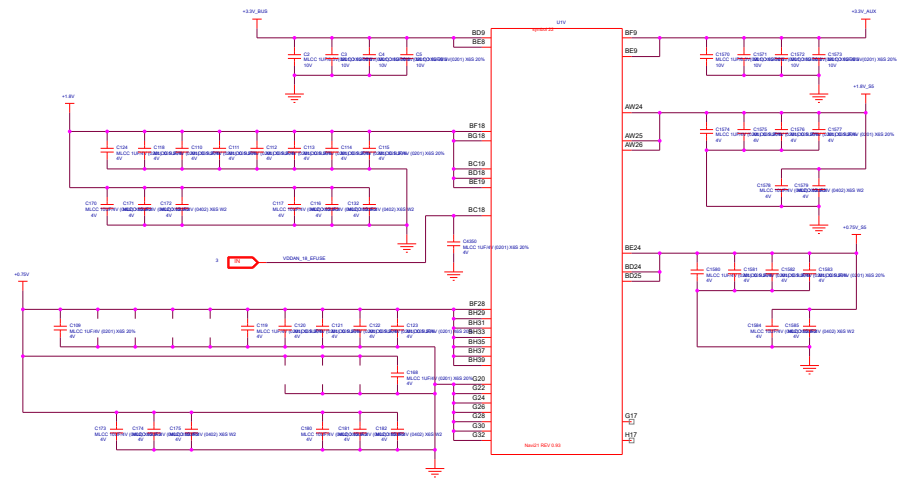
ASUS Re-design logo
Do not place this on reference board

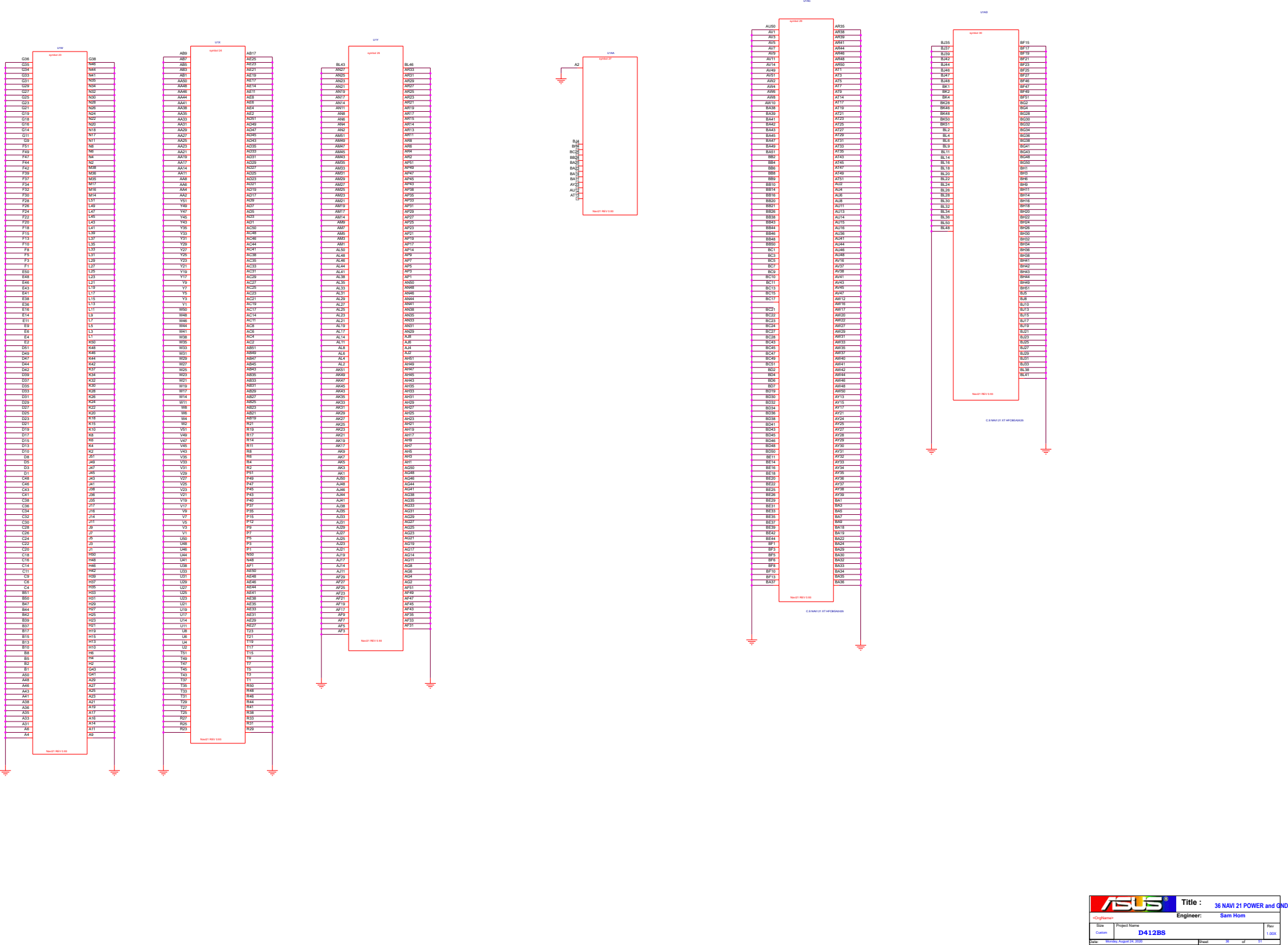








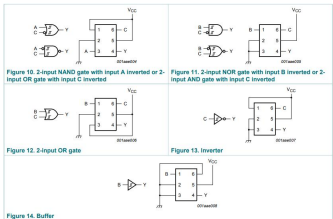




Modify by Scott
Delete QC1112/QC1113/QC1116/QC1114/QC1115/UC1119

Modify by Scott

Delete UC1110/UC1111/UC1112/UC1113/UC1114
UC1115/UC1116/UC1117/UC1118/UC1119



Modify by Scott

Delete QC1116/QC1117

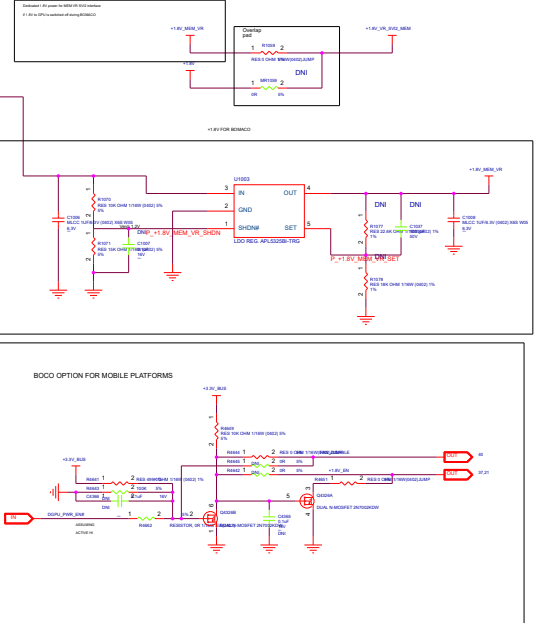
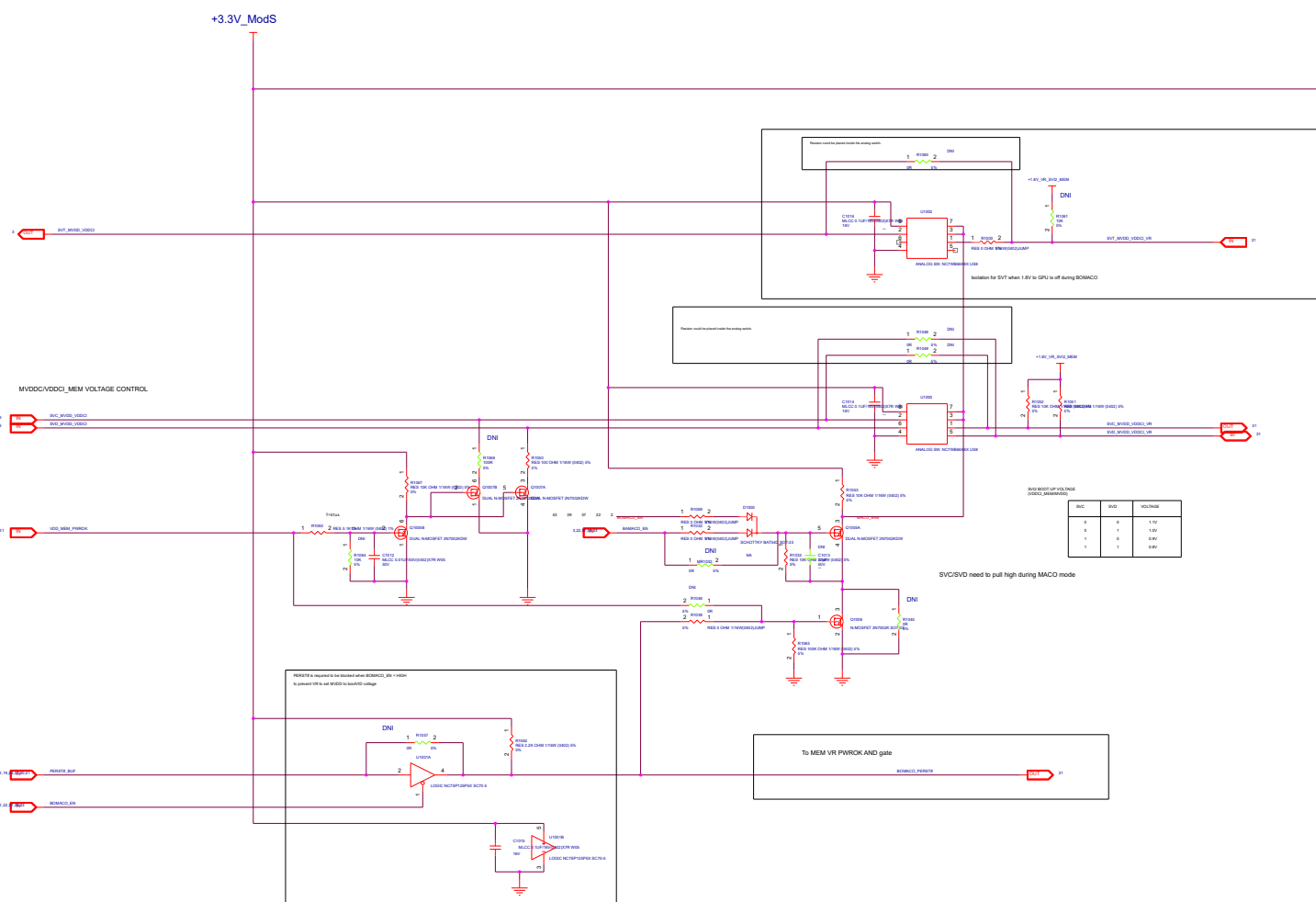


Table 3 Power Rails Status at BAMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN * EFUSE	EFUSE	ON
VDDCR_S5	USB	ON

Table 3 Power Rails Status at BOMACO Mode

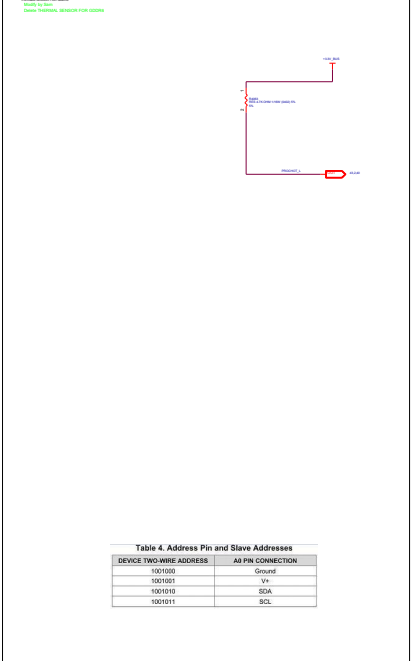
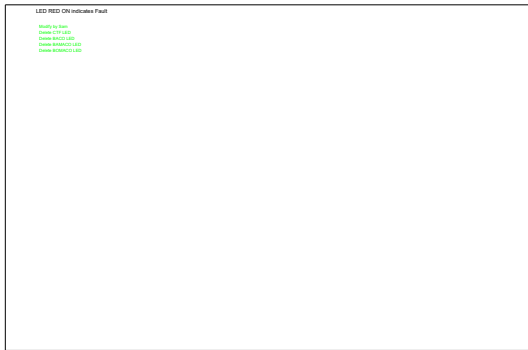
Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN * EFUSE	EFUSE	OFF
VDDCR_S5	USB	ON

Table 4 Key Signals at Different PM Modes

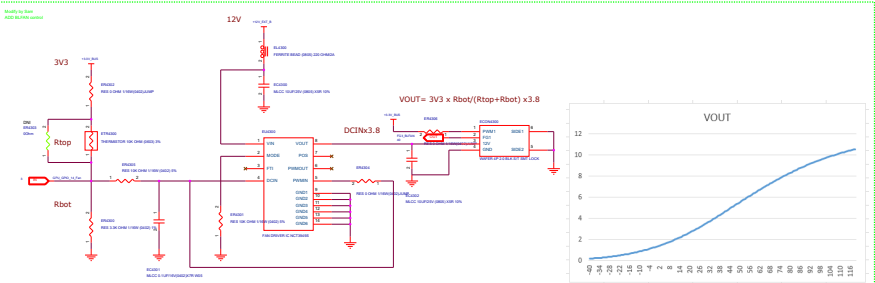
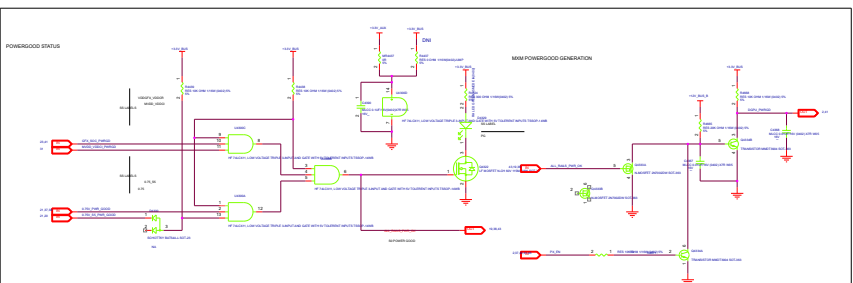
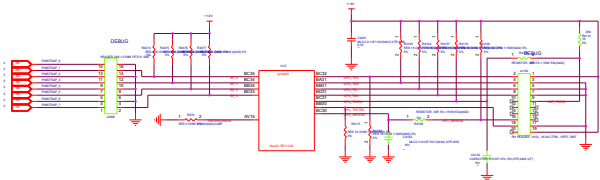
Signals	Default	BOCO	BOMACO
PX_EN	LOW	N/A	N/A
MACO_EN	N/A	N/A	N/A
PERST	HIGH	1->0->1	1->0->1
PWR_EN	HIGH	LOW	LOW
BOMACO_EN	LOW	LOW	HIGH

Table 5 Platform to Support BOMACO

BOMACO_EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID

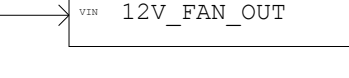
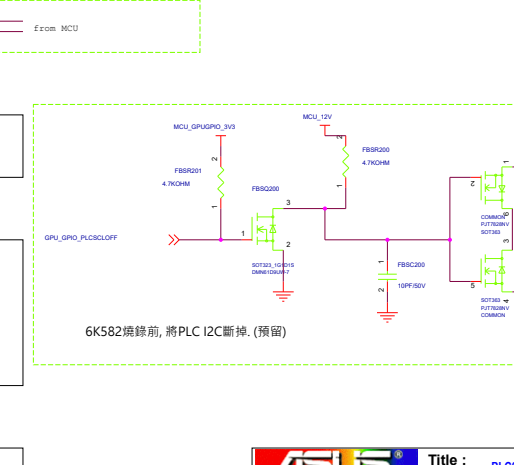
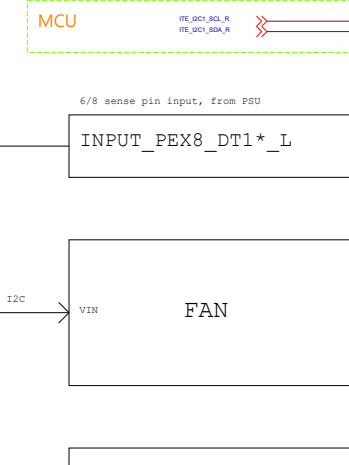
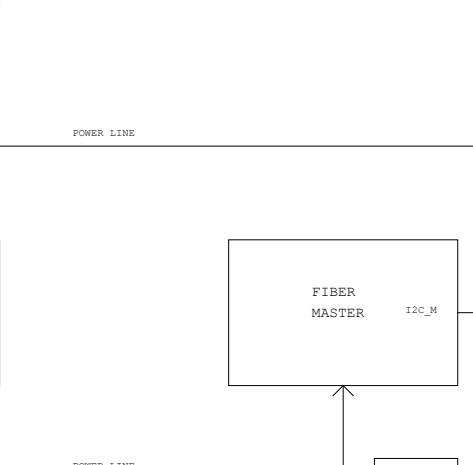
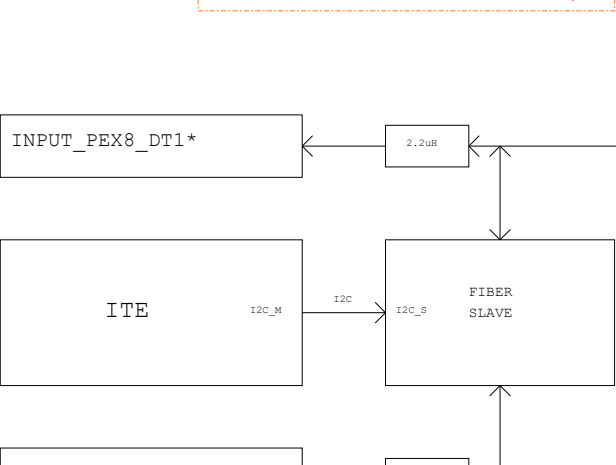
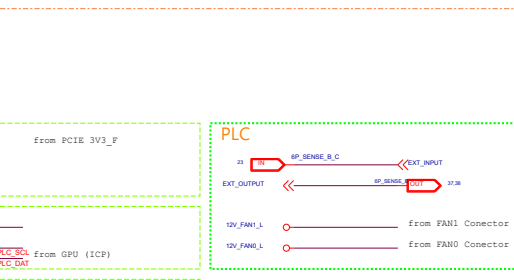
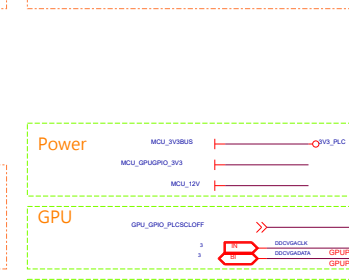
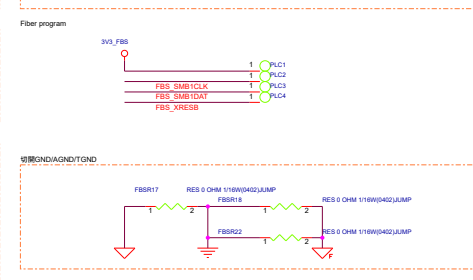
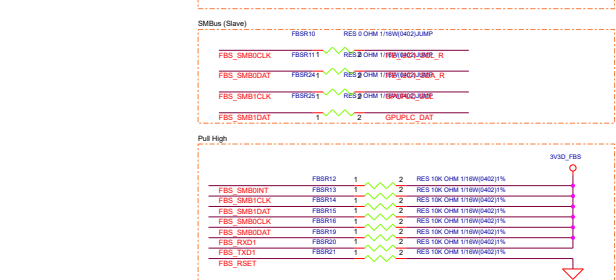
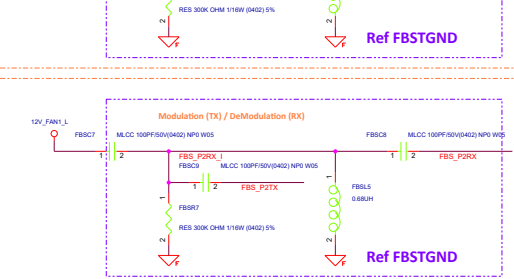
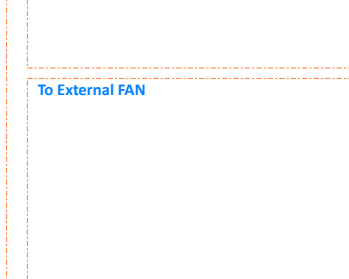
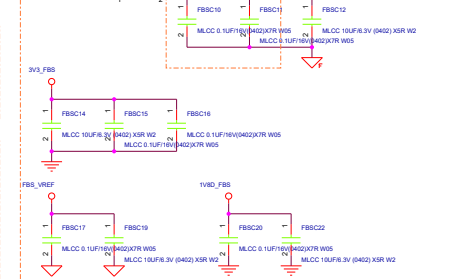
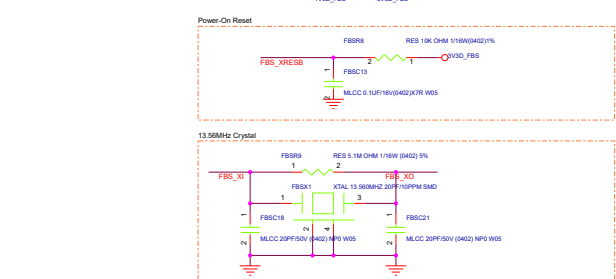
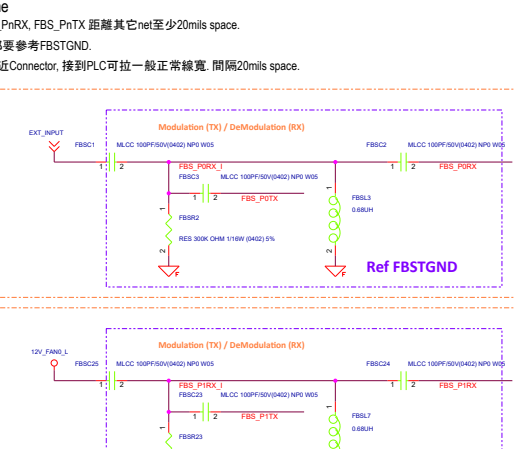
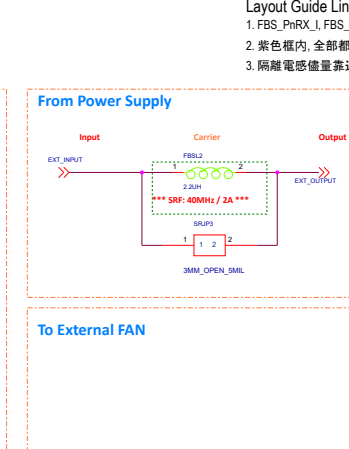
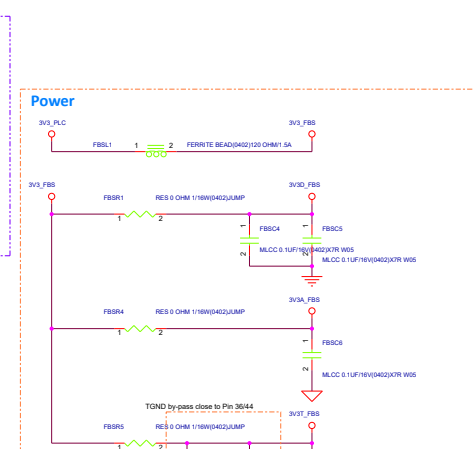
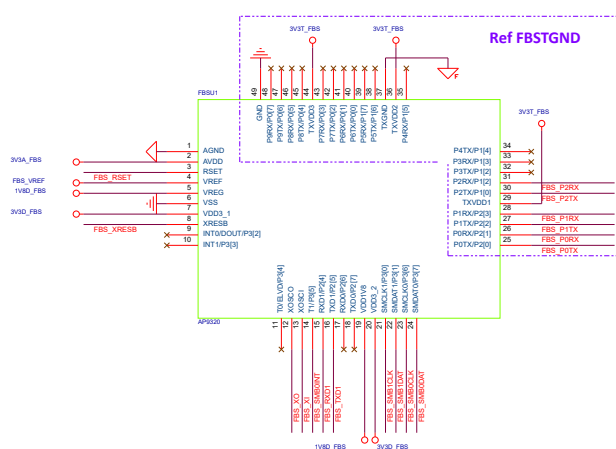


DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL



Layout Guide Line

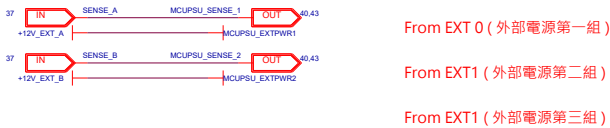
1. FBS_PnRX_I, FBS_PnRX, FBS_PnTX 距離其他net至少20mils space.
2. 紫色框內, 全部都要參考FBSTGND.
3. 隔離電感儘量靠近Connector, 接到PLC可拉一般正常線寬, 間隔20mils space.



Power



PSU DETECT INPUT

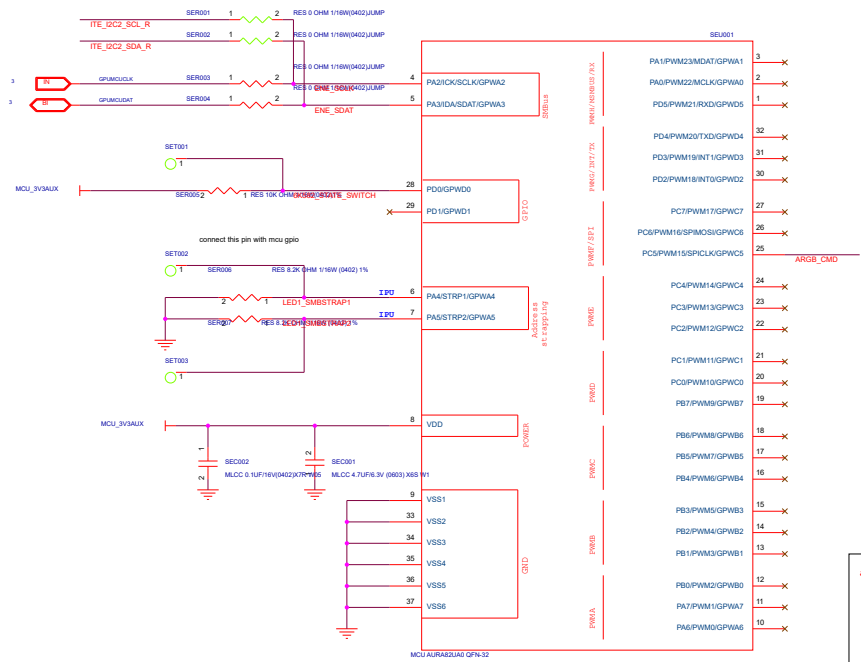


I2C

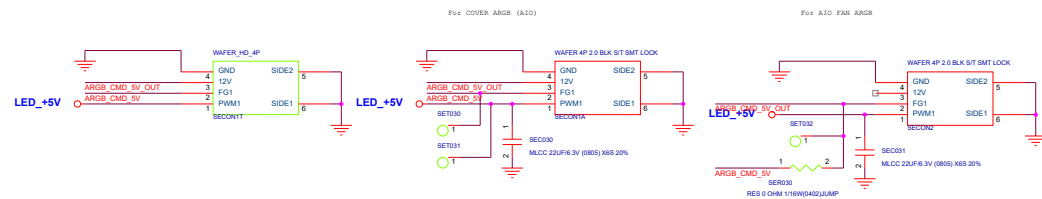


GPU_GPIO

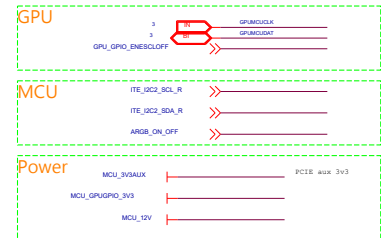
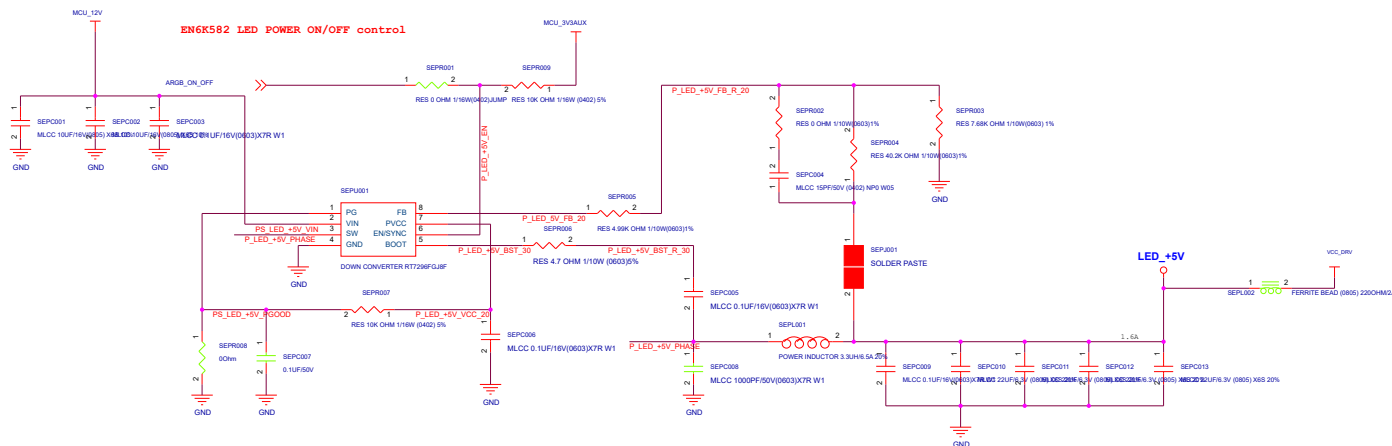




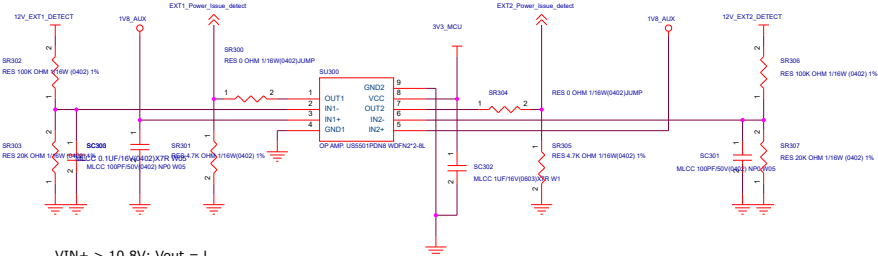
argb connector



ENGK582 LED POWER ON/OFF control



EXT1


 $V_{IN} > 10.8V: V_{out} = L$
 $V_{IN} < 10.8V: V_{out} = H$
 $10.8V \times 20Kohm / (100Kohm + 20Kohm) = 1.8V$

SR301/SR311, 若僅需做一組連接座偵測, 其他零件可以移除, 但SR301/SR310/SR328需上件4.7K



MCU_3V3AUX

pcie 3v3 aux

3V3_MCU

MCUPSU_EXT1W1

MCUPSU_EXT1W2

EXT12V INPUT

EXT POWER connected DETECT PIN



OUPUT: AS ITE8915 INPUT

EXT1_Power_Issue_detect

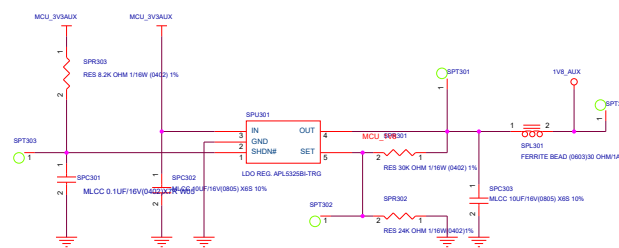
EXT1_Power_Issue_detect

from ite8915

ITE_EXT1_ISSUE_LED

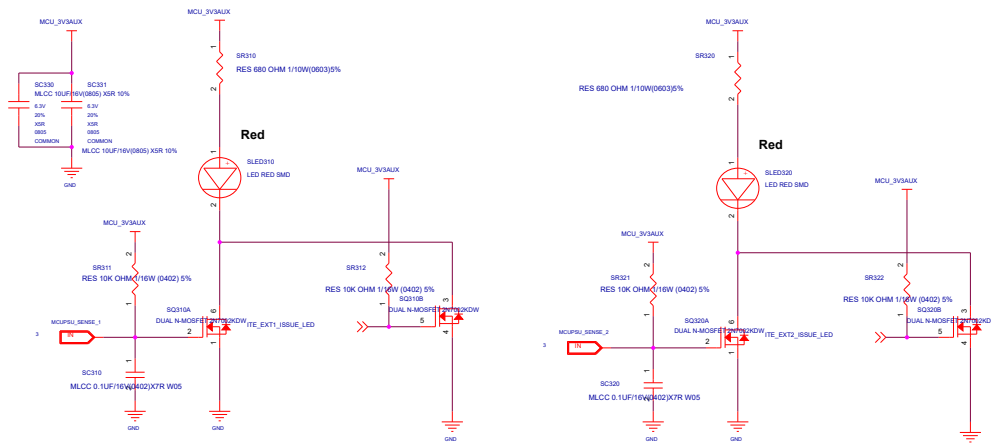
ITE_EXT2_ISSUE_LED

1v8_ref



$$V_{out} = 0.8 \cdot \left(1 + \frac{R1}{R2} \right)$$

$$0.8 \times (1 + 30K/24K) = 1.8V$$



1.EXT power is not connected,
the led is always on
2.EXT power is connected
EXT 12V is over 10.8V, the led turns off
EXT 12v is below 10.8v.the led blink